PSONIX DESIGN GROUP
HVR-1000 Home Video Router System

EEE 193A Section 02 Group 03
Dennis Dahlquist, P.E.

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1.0 EXECUTIVE SUMMARY

1.1 Project Summary

The Psonix Design Team has created a Home Video Router (HVR) system that will enable multiple viewers to watch different or similar video feeds on television sets in separate rooms of the same house. All input signals are fed to the same central location and routed inside of a box at that location before being fed out again to the system users. Thus, each room in the house can have access to all the available video sources without the hassle of extraneous boxes, wires or cables per television. Using the HVR-1000, it is just as possible for all television sets in the home to view the same output source simultaneously as it is for all of them to view separate and distinct outputs at the push of a button. The conceptual product is very useful and practical to the general public. We have reviewed the market availability of products like the HVR-1000 in functionality, and have come to the conclusion that there is a space in the market for a private home-based video routing system.

During the first stage of the project, we laid out the schedule for our engineering team, broke down the workload, named tasks, and defined the length and scope of each individual task. We completed the second phase of the project on schedule, in December 2002. Later in this report, we will provide the details of the operation, along with the progress for each stage of the development of the HVR-1000. During the first stage of the project, it was our purpose to fully design and test our system using simulations, PSPICE, and individual component testing, in the second portion of the project, we aimed to breadboard the entire project, and design the PCB to fit the working product. No project is perfect, and unpredictable problems have arisen frequently and with stubborn regularity. In order to deal with this we scheduled, between tasks, weekly design review meetings, where we sat down and discussed our current state, our remaining goals, and how to deal with the obstacles that had arisen. The results of these team reviews have directed our research and decisions over the last year.

As of May 2002, (last semester), the majority of the non microprocessor dependant modules of Psonix's HVR-1000 were working. We successfully decoded an infrared input (red laser), and sent control signals over a wireless link to simulate controlling of system gain and selection of the different op-amps in the router. We had two analog video paths set up through the router, and were using the IR link/control to select between them in turn. We also refined the router layout to the point where we were comfortable enough to begin PCB layout and design. Programmable logic modules (microcontroller or FPGA) were the only missing item to obtain a working prototype of the HVR-1000.

Each team member completed several design verifications over the course of our first project stage. We verified the usefulness of logic controls as a selector, we verified the ability of filters to solve some of our signal distortion problems, and we verified the ability of IR to trigger wireless transmission of command data at a reasonable bitrate. Also, we developed a reasonable method of switching selections via an IR pulse, we developed a way of using MOSFETs as on-off op amp drivers, and we learned certain things about several parts and devices that have allowed us to make better decisions regarding our system.

Those critical tasks which were absolutely essential to the success of the HVR-1000 are given a brief discussion in this section. These items were at the very base of the project, and had to be completed in order for our system to succeed. They were not always items related to physical problems with the system, but were more often decision items that needed to be resolved before progress could be continued in a given direction. During the first phase of the project, we ran into several of these issues that had not even come up during the initial planning stages.

After internal discussion among the group members last semester, the following action items were placed on Psonix's "top priority list" to be resolved before anything else:

Determine Router Signal Type:

It was necessary to determine whether to use channel 3 as our standard for internal routing, or to perform all signal routing at baseband (with demodulated signals). After more basic experimentation with actual video and passing multiple signals through amplifiers to a single output, we were able to decide that it is easier to use channel 3 as a medium for transmission in our project. The final project reflects this decision.

Develop IR Remote Selection:

It was considered necessary to have a working remote control with the system that sends function-specific IR commands to the router for interpretation. However, after some initial fooling around with different methods of IR transmission and a very primitive remote control setup at the end of last semester, we decided just to transmit selector commands backwards over coaxial cable.

Incorporate Microcontroller & Software:

This was to be the largest step for the project, but it turned out to be the least of our worries at the end. The microcontroller was to detect sequence commands from the selector, decode and remodulate the sequence commands, and control the gain of the op-amps in the selector. The microcontroller was one of the ever changing pieces of our design, constantly being rethought for a "better" configuration. In the end, microcontroller integration went very smoothly.

Modify Filtering For Clean Router Output:

After several filtering iterations, we have produced a VERY clean signal at the output of our system that remains stable for frequencies up to 750MHz. The filtering capacity of our system is one of the things that we are most proud of.

Currently, we have produced a working system that successfully draws multiple video sources into a central router/controller, and distributes them to two television sets simultaneously. It is possible at each of the television sets to switch independently of one another between the video sources offered by the router.

The remainder of this document contains everything we have accomplished, planned, drawn out, designed or completed as it is related to our project. The report also includes our goals, design characteristics, specifications, tests, results and conclusions. All the diagrams, charts, notes, documents and calculations that have provided any use to us in the design of the HVR-1000 shall be included in this project report.

1.2 Resumes

Included on the following pages are the Psonix Design Team member's resumes:

Jason M. McLachlan

108 Fiddick Ln.
Grass Valley, CA 95945
Voice: (530) 273-8619
Fax: (530) 274-1428
e-mail: jmclachl@pacbell.net

Objective

To obtain a challenging position as a Systems Engineer and to become an integral part in the development of hardware, firmware and software.

Work Experience

March 2000 to Present	*Engineer, AJA Video Systems, Inc.* Systems design, development and debugging of professional broadcast video products. Job functions include microcontroller coding, FPGA design, and development of supportive analog and digital circuitry. Design tools include MPLab, Viewdraw, Verilog, and PSPICE. Follow SMPTE and EBU video standards.
March 1996 to March 2000	*Engineering Associate, TDK Systems, Inc.* Responsible for the detection and the follow-through of corrective action for product deficiencies in communication PCMCIA products including modems, ISDN cards, 10/100base-T Ethernet adapters. Worked with ITU-T and Bell data communication standards. Job tools included logic analyzers, FFTs and oscilloscopes.
January 1996 to December 1998	*Self-employed Firmware Engineer and Electronics Technician.* Development, debugging, and maintenance of firmware for PIC-based microcontrollers used in remote data acquisition modules. Also design, build, test and troubleshoot surrounding hardware.

Education

CALIFORNIA STATE UNIVERSITY, Sacramento 1999-Present (Senior Level)
Continuing student, B.S. Degree - Electronic Engineering
Depth Knowledge in Communication Systems

SIERRA COLLEGE, Rocklin, CA 1995-1999
Associates of Science Degree - Physics

SIERRA COLLEGE, Rocklin, CA 1992-1995
Associates of Science Degree - Computer Integrated Electronics
Emphasis in Computer Science

Other Areas of Skill, Ability and Interest

Network manager/administrator for a company of 25 employees. Past experience as a primary technical interface with corporations such as Microsoft, Gateway, Andersen Consulting, Cisco and others. Extensive use of MS Office products to graphically and verbally document, execute and communicate ideas and acquired knowledge or data. Use of Internet for research, development and optimization of current and future products. Able to quickly troubleshoot and solve very detailed and complex technical problems.

Katarina Miletijev

1100 Howe Ave., Apt# 502, Sacramento, CA 95833 (916) 564-7305 serbcat@yahoo.com

OBJECTIVE

An internship position in Electrical Engineering

EDUCATION

CSU Sacramento, Bachelor Science Degree in Electrical & Electronic Engineering - *In progress* ***08/2000-Present***
Modesto Junior College, Associate Science Degree in Physical Science ***Graduated, May 2000***
Modesto Junior College, Associate Arts Degree in General Education ***Graduated, May 2000***

Engineer-In-Training (EIT) Certificate Certificate No. 113153 ***October 27, 2001***

SKILLS

Communication:
Well developed organizational skills
Excellent management and technical skills
Customer service skills
Strong analytical skills
Excellent mentoring and tutoring skills
Proficient teaching skills

Languages:
Fluently speak Serbian, Russian, and English
Understand: Bulgarian, Macedonian, and Ukrainian

Computer:
Systems: Windows (95/98); Macintosh, DOS;
Software: AutoCAD, MicroSim PSpice, MAXplusII, MS Word, MS Excel, MatLab;
Programming Languages: C, Verilog, MatLab, Debug;

RELATED EXPERIENCE:

Psonix Design ***01/2002-Present***
Designing a Home Video Router (HVR) system that will enable multiple viewers to watch different or similar video feeds on television sets in separate rooms of the same house.

AutoCAD and Engineering Graphics Operator, Turlock Irrigation District (TID) ***Summer 98***
Worked on Geographical Information System project entering data of meters, poles and transformer information from paper maps into the computer, using AutoCAD and made myself available to help other engineers with any other work.

OTHER EXPERIENCE:

Administrative Operation Coordinator Assistant / EEE Department / CSU Sacramento ***05/2001-Present***
Administrative file management, assisting department chair and administrative assistant in preparation of outreach material, updating student records, maintaining numerous spreadsheets, receiving and distributing purchased merchandise.

Russian Translator and Mathematics Teacher Assistant / Mira Loma High School ***08/2000-08/2001***
Part of University Outreach- PAD Program at CSU Sacramento. Assist Russian and Ukrainian students in mathematics and with overcoming language barriers and cultural differences.

Mentor, Educational Talent Search/ Modesto JC & Saturday Scholars / CSU Sacramento ***02/2000-08/2001***
Prepare high school students from low-income families and first generation college students for college. Provide guidance to help students become successful individuals.

ACTIVITIES, HONORS, AND LEADERSHIP:

- Fully supporting myself and my sister while in college, working 20 hours a week while carrying a full course load, and maintaining an overall GPA of 3.5 — Fall 1997-present
- Dean's Honor List / CSU, Sacramento — Spring 2001-present
- Golden Key International Honor Society, Life Time Member — Fall 2001
- Tau Beta Pi Honor Society, Life Time Member — Fall 2001
- Active Member, Society of Women Engineers & Institute of Electrical & Electronic Engineering — Fall 2000-2001
- Alpha Gamma Sigma Honor Society (AGS), Life Time Member — Fall 1997
- Secretary, Teacher Appreciation Dinner & Found Raising Committee Chair (AGS) — Spring 2000
- Ed Walsh Outstanding Service Award-Scholarship (AGS) — Spring 1999

Austin C Roundtree

7853 La Riviera Dr. Apt. 179
Sacramento, CA, 95826

Phone: (916) 381-2698
Email: austin.roundtree@psonix.com

Objective:

To obtain an entry level position in RF or analog IC design engineering.

Education:

In progress: B.S. in Electric/Electronic Engineering
California State University, Sacramento
Expected date of graduation: December 2002
GPA: 3.65 (CSUS)

Related Coursework:

Electronics I & II	Circuit Logic Design	Network Analysis
Signals & Systems	Applied Electromagnetism	Semiconductor Physics
Microprocessors	Modern Communications	Feedback/Control Systems

Technical Knowledge & Skills:

Operating Systems: Windows (98/NT4.x/2000), DOS, Linux, Unix.
Software Skills: C, HTML, Verilog, PSPICE, MaxII++, MATLAB, proficient with MS Office Suite.
Excellent written and verbal communication skills, very strong logical/mathematical background.
Excellent team, organizational, problem solving and analytical skills.

Related Experience:

Advanced Programming Institute, Inc. ***(4/2000 – current)***
El Dorado Hills, CA
Title: Quality Assurance Engineer/Web Designer/Technical Writer

Assisted in the re-engineering, development and testing of Advanced Programming Institute's Object Oriented software products and related educational materials. Provided and reviewed material used in the re-writing of the company's five-day Object Oriented Project Management course manual and class laboratory exercises.

Designed, created and developed the Advanced Programming Institute website. Aided in the creation and review of the website's written content. Responsible for website maintenance, hit analysis, and implementing future developments.

Routinely tested software products for quality and functionality. Responsible for maintaining record of all errors, changes and issues related to software product.

Senior Project Design ***(1/2002 – current)***
California State University, Sacramento (in progress)

Our project group of four is creating a Home Video Routing system (HVR) capable of taking four to six video inputs at a central location and routing them all to different television sets which are distributed throughout the household. A remote control/analog switcher will allow the user to specify which video input is desired at the user's present location.

Personal responsibilities include analog/digital filter design, amplifier design, routine testing, and complex mathematical analysis.

Activities & Accomplishments:

Currently an active member of IEEE.
Athletic by nature, and enjoys a wide variety of sports and outdoor activities.
Enjoys jazz and classical music: an accomplished pianist.

Marck D. Gorszwick

220 Cadillac Drive #18
Sacramento, CA 95825
gorszwim@ecs.csus.edu
(916)-568-1916

OBJECTIVE: Seeking a position in RF Engineering

EDUCATION:

In progress: Bachelor of Science, Electrical and Electronic Engineering; Expected graduation December 2002 – California State University, Sacramento.

Related Courses:

Logic Design	Circuits I/II	Digital Signal Processing
x86 Assembly	Electronics I/II	Modern Communications
Random Signals	Signals & Systems	Wireless Comm Systems
Device Physics	Feedback/Contol	Field Lines/Transmission

SKILLS:

Foreign Languages:
Fluent Spanish (One year exchange program to South America)

Software:
Wireless Design/Optimization, Circuit Design (SPICE), Digital Logic Implementation

Computer Languages:
Verilog, ANSI C, x86 Assembly, UNIX Shell Scripting, SQL, HTML

Operating Systems:
Various UNIX/Linux derivatives, Windows, Mac OS

EXPERIENCE:

Sprint PCS, RF Engineering Intern — **June 2000 – August 2000**
June 2001 – August 2001

- **Optimized maturing CDMA network in dense urban, rural, and residential areas**
- Successfully migrated 50 sites from Sacramento to San Francisco
- Developed system to track unused equipment

Sprint PCS, Indirect Sales — June 1999 – May 2000

- Advocated Sprint service over competition.
- **Consistently exceeded goals. Ranked lead salesman in Sacramento**

US Air Force, System Administrator/Paralegal — January 1995 – August 1998

Installed, configured and maintained client and server network operating systems, including diagnosing system malfunctions, security breaches, and implementing improvements in efficiency and performance. Systems included NetWare, Unix, and Windows based machines

OTHER ACTIVITIES:

- **Amateur Radio Operator**
- **IEEE Member**

2.0 PROJECT DESCRIPTION

2.1 Project and Personal Goals

Psonix's goal is to provide quality and affordable solutions for home video distribution to the average home consumer. More specifically, we wish to design a practical, useful, and affordable device that works to specifications and affords the user an easy and attractive method of distributing and controlling the many video sources available in-home today. Rather than use multiple cables and boxes per television to run video wherever it is needed, we hope the customer will view our device as a tasteful alternative to spending time unhooking and relocating device after device to watch a DVD movie or a cable channel every time they wish to relax and enjoy a media presentation.

As a senior project group this semester, our goals were as follows:

1. *To learn new things*. We all realize that in the real world, you are only as valuable as what you know. The best answers to the hardest problems come from the widest range of experiences, and each one of us in the team wishes to expand our existing knowledge base and learn several new things, as well as hone the skills we already have.
2. *To gain experience in the field of engineering*. The Senior Design Project is a beginner's view into the real world of engineering. We hope that the experience will prove useful to every one of us when we go out to procure jobs in the real world. The experience we get in this project is the experience future employers will look at when they consider us for positions, and we want this project to be as fulfilling as possible.
3. *To develop teamwork skills*. Nothing is as important as teamwork. The members of Team Psonix all hope to learn to work together to overcome difficulties and solve problems, because these skills are what make the difference between success and failure.

Each member of team Psonix has also stated their goals individually.

2.1.1 Jason McLachlan

Wanted to benefit from Senior Project and improve in the following ways:

- I hope to learn as many new things as I can from Senior Project. My goal is to enrich my skills and abilities to design and manage an electronics project.
- I want this project to be challenging and practical. I want to see this project work in the end.
- I want to share as much as I can with my other group members. This is a team effort, and I want to learn as much as I can about teamwork.
- I want my accomplishments from this project will say something good about me.
- I want to become a better analog and digital designer. I would also like to get better at filter design.
- I want to contribute as much from my past experience with a digital and analog design.

2.1.2 Katarina Miletijev

Expected to get the following things out of the project:

- To get an insight of what it is to be an engineer: to design, plan and finish a designed project
- To find out which areas of electrical engineering interests me the most (analog/digital electronics or wireless communications)

- Strengthen my skills (analytical, organizational, written, presentational and team work)
- Gain experience in electrical engineering

Planned to learn the following things:

- To work in a team
- Broaden knowledge of wireless telecommunications
- Learn more about analog and digital design
- Learn more from team members, and develop good teamwork skills.

2.1.3 Austin Roundtree

Personal goals over the two semesters comprising senior project were as follows:

- I wish to significantly further my understanding of RF design, as I wish to pursue a career in wireless communications technology someday. It is my desire to learn more about wireless transmission, modulation, reconstruction, and other processes associated with RF.
- I wish to further augment and develop my existing knowledge of filters and amplifiers by direct application.
- I wish to learn more about system controls, micro-controllers and their functions, coding, decoding and system integration.
- I want to walk away with a firm understanding of the principles and methods involved with real project design and implementation.
- I want to get involved now with as many ideas and concepts as possible so that when I decide to pursue graduate school, I have a foundation to build on, and experience to start with.
- I hope to finish with the confidence that I can go out into the real world and use the talents and abilities honed in senior project to obtain and hold a job in analog design someday.

2.1.4 Marck Gorszwick

Wanted to learn and get the following out of senior project:

- Hopes to learn as many new things as possible from Senior Project. Plans to enrich his current skills and abilities in designing and working on an electronics project.
- Wants the project to challenge his abilities and set him interesting goals.
- Wants to share as much as possible with all other team members and develop good teamwork skills and abilities.
- Wants the project to be an accomplishment he can be proud of, and show off in future job interviews.
- Wants to become a better RF engineer and increase his current knowledge of the subject so that he has a better chance of getting a job in RF engineering someday.
- Wants to contribute as much as possible from his past experience in wireless communications.
- Hopes to walk away satisfied that he has done everything he could to make the project a good one, and hopes to be proud to mention the project to others in the future.

2.2 Team Work Breakdown

In accordance with our initial team contract, we had agreed to break down the project workload into sections and assign specific areas of responsibility to each member of the project group. These areas of proficiency were assigned according to the individual's previous experience and education as well as preference. The complete work breakdown is outlined further below.

As of the fourth week of the first semester, the work breakdown had generally been decided as follows, each team member to his or her better skill areas. However, several modifications were made to accommodate changes made over the course of the second semester. With the portions of the project relating to wireless transfer removed, the overall workload was more equally distributed to include new and exciting challenges.

2.2.1 Work Breakdown:

- *Jason McLachlan*; Video Analysis, Systems Design, PCB Layout.
- *Austin Roundtree*: Analog Design, Mathematical Analysis, PCB Layout.
- *Marck Gorszwick*: Filter Design.
- *Katarina Miletijev*: Digital Design, Telecommunications.

Since all of us in the team wished to learn something new about each new component going into the project, most of the tasks and events passed through the hands of all project members in turn. Most of the time, project tasks were distributed evenly across the group, just to ensure that each team member was able to understand the project status and any results for individual components of the overall project. As such, we were able to learn as much from each other inside of the group, while maintaining some individuality in ideas. In general, our group members had enough knowledge overlap to allow us to solve most issues together. Generally speaking, the responsibilities of each group member involved those tasks most similar in nature to that person's area of expertise. A better description of each person's skills is itemized below:

2.2.2 Responsibilities:

- *Jason*: Responsible for overall router design, digital and analog component placing, soldering, prototyping, microcontrollers, component selection and major decision making.
- *Austin*: Responsible for analog design, filter design, filter networks, op amp design, impedance matching, software, mathematical analysis and mechanical construction.
- *Marck*: Responsible for wireless design, IR components, RF components, PLLs, software coding and modulation/demodulation.
- *Katarina*: Responsible for digital communication and wireless design, logic design, modulation/demodulation, digital encoding/decoding and RF design.

2.3 Concept Diagram

Figure 1-1 below shows the concept diagram of our product. The user can see how the video selector unit is used at each television set to select between the multiple inputs. The input from each selector runs commands back to the main box, labeled "Video Router" in the figure. This is where the actual routing occurs. The chosen input is then routed to the specific television set via the proper video feed. (The technical details of the system are discussed further in the next section.)

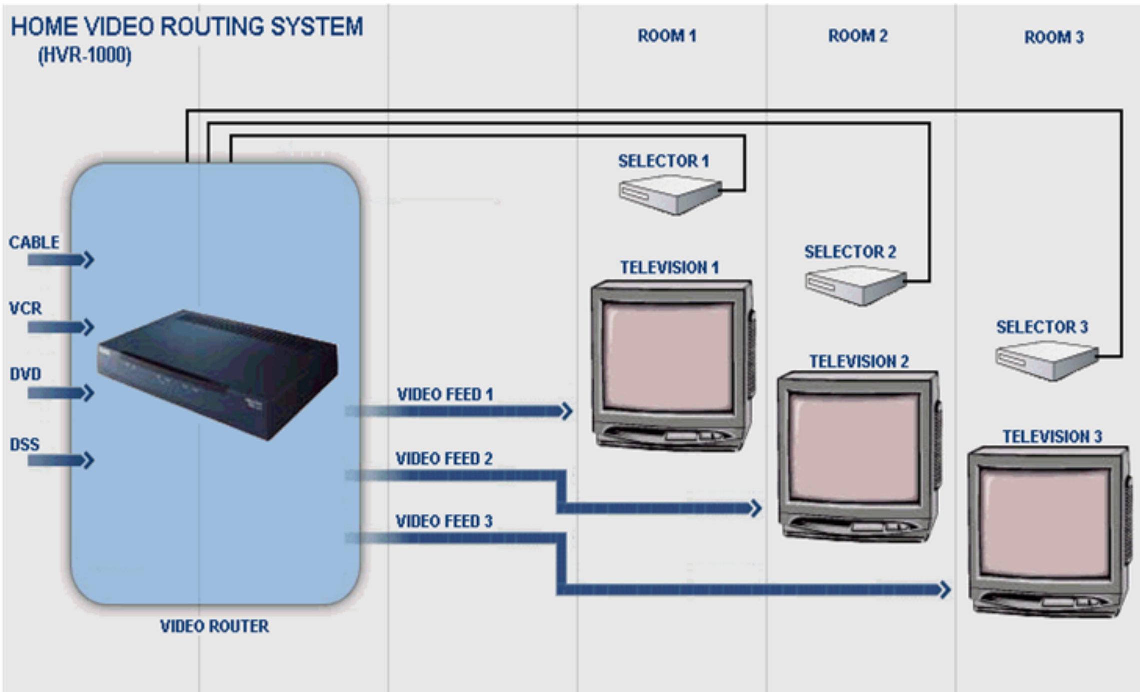

Figure 1:: Concept Diagram

2.4 Functional Description

The concept of a video router is nothing new – casinos and security users have used them for several years to dynamically route video to multiple locations simultaneously. This simple concept has been slow and poorly implemented in home the home market though – in its most familiar form, people with more than one television were forced buy multiple VCRs or DVD players to watch movies in multiple parts of the house. Also common was the use of A/B switches to allow the coaxial cable to send the output of the DVD to another room.

Psonix's design goes one step beyond the A/B switch by providing intelligent routing at the media hub. With our flagship product, the HVR-1000, home users can now have any video source displayed on up to four televisions simultaneously. Moreover, inputs and outputs can be dynamically switched to allow full utilization of the user's entertainment system.

The HVR-1000 has four video inputs, and four video outputs, with a microprocessor controlled switching facility to control the system's output. Unobtrusive remote units reside at each television to allow control over the HVR-1000 routing table, and provide a means to conveniently relay IR commands back to the media hub associated components, allowing complete viewing control from any connected room in the house.

2.4.1 What HVR Does:

HVR takes in 4 video inputs, and independently routes them to 4 video outputs. Switching in the router is controlled remotely via selector stations that relay IR commands from a remote control directly to the router.

The video signals entering and leaving the router optimized for on channel 3, however in while finalizing the design of the product, we chose to include analog muxes that allow up to 750 MHz of bandwidth (ie, the full VHF/UHF spectrum) to be transmitted. The primary HVR box is transparent to the incoming video signal. The video signals are terminated, buffered, , filtered, and routed by this box. All signals leaving the box have proper source impedances. Devices such as DVD players, DSS receivers, and any other video source modulated for channel 3 meet the requirements for the HVR-1000. Because most consumer video appliances already meet these requirements, nearly everyone can use this device.

2.4.2 What the HVR Does Not Do:

Because demodulation circuitry is not included on the router, it is only possible to pass frequencies up to 750 MHz through the selector. As such, using the HVR for relaying raw DSS signals (ie, above 1 GHz) , or as an extender for ISM applications is not possible. Additionally, the HVR-1000 does not have any facilities to modulate baseband video. As such, it is not possible to connect a video device without a modulated source directly to the HVR.

2.4.3 Target User:

HVR is designed for the consumer market. Anyone who wants to share a single set of video devices throughout a household will want this device. For example, instead of having to buy a separate DSS receiver for each television set in the house, the output of one DSS receiver can be routed anywhere in the house. As well, instead of dealing with several wires, antennas and cables per television set in the house, video selection at each television in the household can be controlled by a single cable and a single selection unit.

2.4.4 How It Works:

All of the video equipment is centrally located and controlled via continuous in band tone control. A receiver at each television set captures remote control commands. These commands are then sent to the router for processing. An onboard sequence detector decides whether or not these commands are for the router. If they are determined to be for the router, the commands are forwarded to the intended video device via an RS-232 link. The RS-232 signals are converted into IR and sent directly to the target video source.

2.4.5 What's In It:

A mixture of analog and digital components is implemented in this design, including opamps, filters, microcontrollers and FPGA's. This design leaves room for many expandable ideas, including wireless control, and on-screen display. Psonix hopes to expand its product line someday to include newer versions of the product with increased functionality. We tried to keep this in mind while firming up and threshing out our actual design. To accommodate this additional functionality, we added several features to the router board that would make the development and addition of features easy to provide. Added were facilities for the microcontroller, FPGA, and CPLD to be used for a variety of applications over the course of future offerings by Psonix. Eventually, as our product line becomes more mature, these development features will be removed for added cost savings to the consumer.

3.0 PROJECT SPECIFICATIONS

3.1 Specifications

Following, you will find the full specifications for the Psonix HVR-1000 Home Video Router. Each specification heading included below has values for both the router box itself and the video selection unit included with the device.

Project specifications include those for system inputs, system outputs, system control, signal accuracy (as regards attenuation) power requirements and operating specifications, as well as actual measured device dimensions.

3.1.1 Inputs:

Router

- Voltage: 700mV video, 300 mV sync.
- Impedance: 75 Ω.
- Type: F type connector.

Receiver

- IR receiver.

3.1.2 Controls:

Router:

- Controlled through continuous in band signaling for designation of input frequency.
- FPGA/CPLD interprets IR commands to be relayed to remote devices.

Receiver

- FPGA to generate tone/input selection.
- IR receiver to listen for commands to relay.

3.1.3 Outputs:

Router

- 1V pp RF carrier.
- 75 Ω output impedance.

Receiver

- Hardwire control to router for in band frequency notification/video downstream.

3.1.4 Accuracy:

- $\pm$ 1dB from input to output

3.1.5 Power Requirements:

Router

- 15W (120VAC @ 125mA)

Receiver

- 2W (120VAC@ 16.7mA)

3.1.6 Operating Environment:

- 0-50 $^\circ C$
- <80% humidity
- <5000 rads ☺

3.1.7 Other Dependent Specifications:

Router

- Weight: Less than five pounds
- Size: Max dimensions 8x12x4 (LxWxH)

Receiver

- Weight: Less than two pounds
- Size: Max dimensions 6x6x2 (LxWxH)

3.2 Product Features

The HVR-1000 is a highly versatile product with several key features and attributes that include the following:

- Four standard coaxial video inputs to which the user can connect virtually ANY video device or standard with coaxial transmission capabilities, including Cable, Digital Satellite, VCR, DVD and many digital cameras and recording devices.
- Four standard coaxial outputs that the user can connect directly to the back of any standard television set.
- Direct routing capabilities that allow as many as four different television sets to view the same video input simultaneously or all television sets to view separate channels without cross-talk or intermodulation between signals.
- A selector box for each television set that allows the user to change between router inputs per viewing station.
- A IR configuration on the front panel of each selector box that allows the user to easily change input channels by simply pressing a predetermined sequence of commands to change inputs, or by sending specific IR commands to the router for interpretation.
- An IR relay function that sends pertinent remote commands over the house wiring to the specified device so the user can change VCR or DVD settings without getting up and walking into the other room.

Home Video Router 1000
Instruction Manual

4.1 Introduction

Congratulations on your purchase of Psonix's flagship product, the HVR-1000. We appreciate your business, and hope you'll recommend our products to your friends and family members.

The HVR-1000 is the only product available on the market that allows you to choose what video input you want to view (VCR, DSS, DVD, CABLE), and where you want to view it. Its simplified design and sleek contouring provide an attractive addition to any home entertainment system. Additionally, the HVR-1000 offers the unique ability to forward remote control commands from any equipped selector box to your entertainment center, providing complete convergence for all your home video needs.

The HVR-1000RS comes packaged with one main unit for your entertainment system (HVR-1000R), and two selector units (HVR-1000S) for your remote televisions. Additional selector units can be purchased directly from Psonix, or your Psonix authorized retailer.

Your HVR-1000RS box should include the following:

- HVR-1000R – Video Router
- 2 HVR-1000S – Selector Boxes
- RG-8 patch cables
- Power Supplies

Optional Accessories (must be purchased separately);

- HVR-1000i – Infrared extender cable

4.1.1 Before You Begin:

Installation of the HVR-1000 was designed to be simple, however, reading the complete instruction manual before installing is recommended to ensure maximum effectiveness of the product.

There are a couple things to keep in mind before your HVR-1000 is operational. Primarily, the HVR-1000 uses traditional coaxial cable to transmit the signal from your entertainment system to the remote television. If you don't already have cable between the two locations, you will need to run one. *This may require drilling holes, and may require the advice of an electrician.* Additionally, should your cable runs be in excess of 100 feet, you may require an in line amplifier to boost the signal. Such devices are available from your local electronics retailer.

The average installation time for a house with three connected televisions is approximately 2 hours.

4.1.2 Items Required For Installation:

- Drill
- Pliers
- Screw Driver
- Screws
- Cable filling caps
- Coaxial Cable (type RG-6/RG-8 preferred)

4.2 Project Diagram

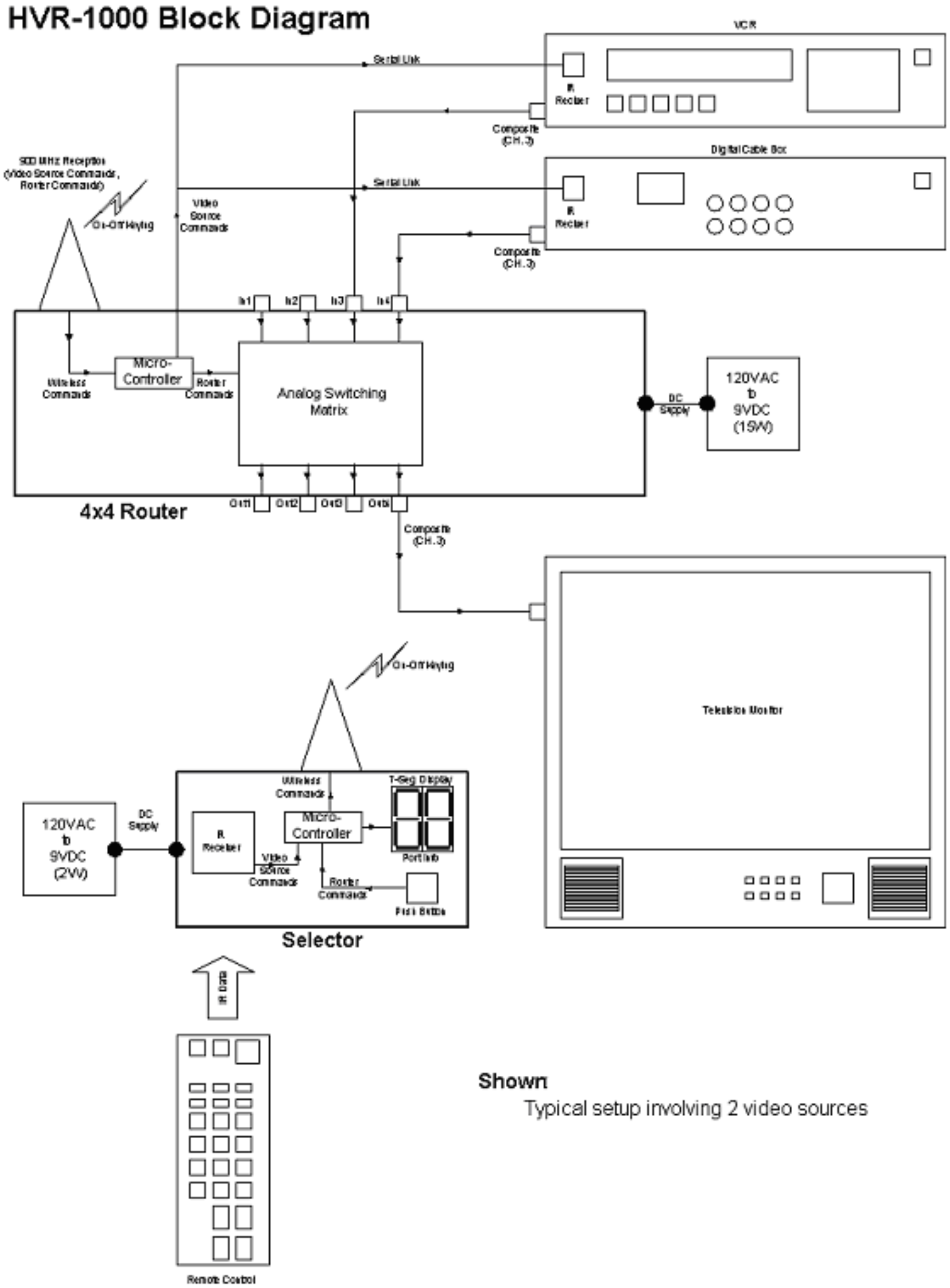

Figure 2:: Project Diagram

4.3 Installation Instructions

To begin the installation, remove any unpacked devices from the packaging box, and store the box should you ever need to return the unit for service.

4.3.1 Setting Up The HVR-1000R:

The HVR-1000R is the heart of your new entertainment accessory, responsible for changing the inputs from your DVD, DSS, Cable, or other alternate accessory that provides a channel 3 output. Before connecting any of your devices to the router, the tips of your video cables should be cleaned with an ear swab and rubbing alcohol to guarantee that the highest quality signal is transmitted.

After the HVR-1000R has been unpacked, and the tips have been cleaned, the device is ready to be connected. The diagram in section (3.2) above shows a detailed illustration of the proper installation of the HVR-1000R.

If you purchased a HVR-1000i, the infra-red extender cable, you may plug it into the port labeled "IR" on the rear of your HVR-1000R.

Make sure that the router is seated in a secure, stable location, and that the front is cleared of any obstructions, as they may interfere with the normal operation of the remote relay functionality of your HVR-1000.

4.3.2 Setting up the HVR-1000S:

As mentioned in the introduction, you may need to drill holes from the router to the selector. Before drilling, you should be aware that serious injury or death can result from drilling without detailed knowledge of your home's wiring. Additionally, modifications to an apartment may require approval from your management.

The tips of the coaxial cable should be free from grime and dirt before you connect them to your HVR-1000S, as a clean connection will ensure that you receive the highest quality video on your television set.

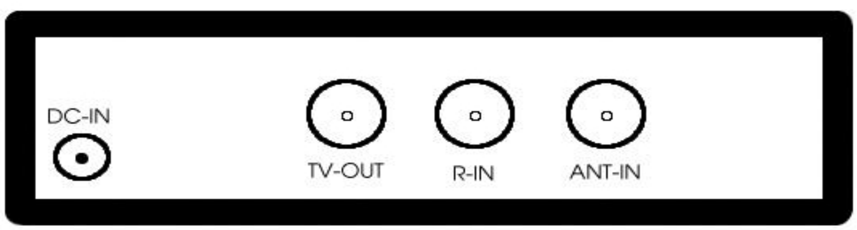

Figure 3:: Selector Box Rear Diagram

Attach the cable from your HVR-1000R to the R-IN port on the rear of the selector. If you have an external antenna that you'd also like to use with the television, you can connect it to the ANT port.

Run the DC adapter from any wall plug to the back of your HVR-1000s and plug it into the DC-IN port. This cable gives power to your video selector.

After connecting your HVR-1000S to your television, your system is configured, and ready to be tested.

4.4 System Operation

In order to have multiple outputs working, you'll need to set the station ID for each selector box in your house. To set the station ID, rotate the knob on the rear of the selector to an unused number, and test the system operation by pressing the source selection button.

Figure 4:: Selector Face

Changing inputs only requires you to push the button on the front of the selector once. If the channel does not change when the button is pressed, you may be out of range, or the system may be malfunctioning. To increase the range of your system, you can purchase the HVR-1000A, the external antenna.

Figure 5:: Selector Face After Increment

An additional feature of the HVR-1000 is the ability to forward remote control commands from any selector box to the router. You can disable this feature at any time by changing the IR switch to OFF (or placing a small piece of electricians tape over the IR receiver.) Note: you may wish to turn this feature off if you have several models of the same television or VCR in both the selector and router rooms.

Note: The HVR-1000 is designed to be powered at all times. Should you experience a power failure, the unit will loose its memory, and all inputs will be reset to the primary input.

4.5 Troubleshooting

Problem	**Cause**	**Solution**
Unit does not power on	Not plugged in, fuse blown	Check power supply and connections, replace fuse
Video not received at selector	Cable not connected securely/cable bad	Test cable connection, replace if necessary
IR Commands not relayed	Router/Selector IR port blocked	Clear obstructions at Router or Selector
Input channels not changing	Interference	Move Router/Selector to area with less interference

4.6 Warranty

Psonix Corporation will repair or exchange your HVR-1000 router or selector free of charge in the event a defect in materials or workmanship with a new, or comparable remanufactured unit in exchange for the defective unit for a period of one year after the original date of purchase. Psonix Corporation disclaims any liability for consequential damages as a result of misuse or abuse. In no event will Psonix Cooperation be responsible for any amount of damages beyond the amount of the product at retail.

This warranty is extended only to the original purchaser. A purchase receipt, or other proof of date of original purpose will be required before warranty performance is rendered. This warranty only covers failures do to defects in materials or workmanship which occurs during normal use. It does not cover failures which are caused by products not supplied by Psonix Corporation, or failure which result for accident, misuse, abuse, neglect, mishandling, misapplication, alteration, faulty installation, modification, service by anyone other than our factory service center, or damage that is attributable to acts of God, war, or extraterrestrial invasion.

Additionally, the following are not covered, and in fact void the warranty: Connection of wrong power supply to unit, attaching high voltage input/output to the router. There are no express warranties except listed as above.

Psonix Corporation and any reseller thereof, shall not be liable for incidental or consequential damage resulting for the use of this product, or arising out of any breach of this warranty. If a problem with your HVR-1000 develops during the warranty period, call Psonix Corporation at 800-432-2388.

4.7 Technical Specifications

Power (Router)	*15 W*
Power (Selector)	2 W
Input Voltage (peak/peak)	700mV Video 300mV Sync
Output Voltage (peak/peak)	700mV Video 300mV Sync
Input Impedance	75 Ω
Output Impedance	75 Ω
RX Frequency	Channel 3 (freq?)
TX Frequency	Channel 3 (freq?)
Video Formats	NTSC SECAM PAL
Maximum Frame Rate	
Maximum Bandwidth	
Operating Temperature	55° C
Accuracy	+/- 1 dB
Net weight (router)	< 5 lbs
Net weight (selector)	< 2 lbs
Dimensions (router)	8x12x4" (L, W, H)

Power (Router)	*15 W*
Dimensions (selector)	6x6x2 (L, W, H)
Fuse (replaceable)	1 A
Ambient Radiation	< 5000 rads/meter

4.8 Contact Information

Psonix Corporation maintains an active web page, with up to date information about upcoming products, investor relations, technical documents, and employment opportunities. Should you need to reach us, please use the following addresses:

General Correspondence:

Psonix World Headquarters
44 Montgomery Ave, Floor 86
San Francisco, CA 94102
(415) 232-2932
www.psonix.com

Warranty/Technical Support Service:

Psonix Repair
PSC:HVR1000
1338 Paseo Padre Ave
Freemont, CA 94538
(800) 432-2388
www.psonix.com/support

5.0 PROJECT TECHNICAL DETAIL

5.1 Block Diagram

Shown below are the system block diagrams for the HVR-1000:

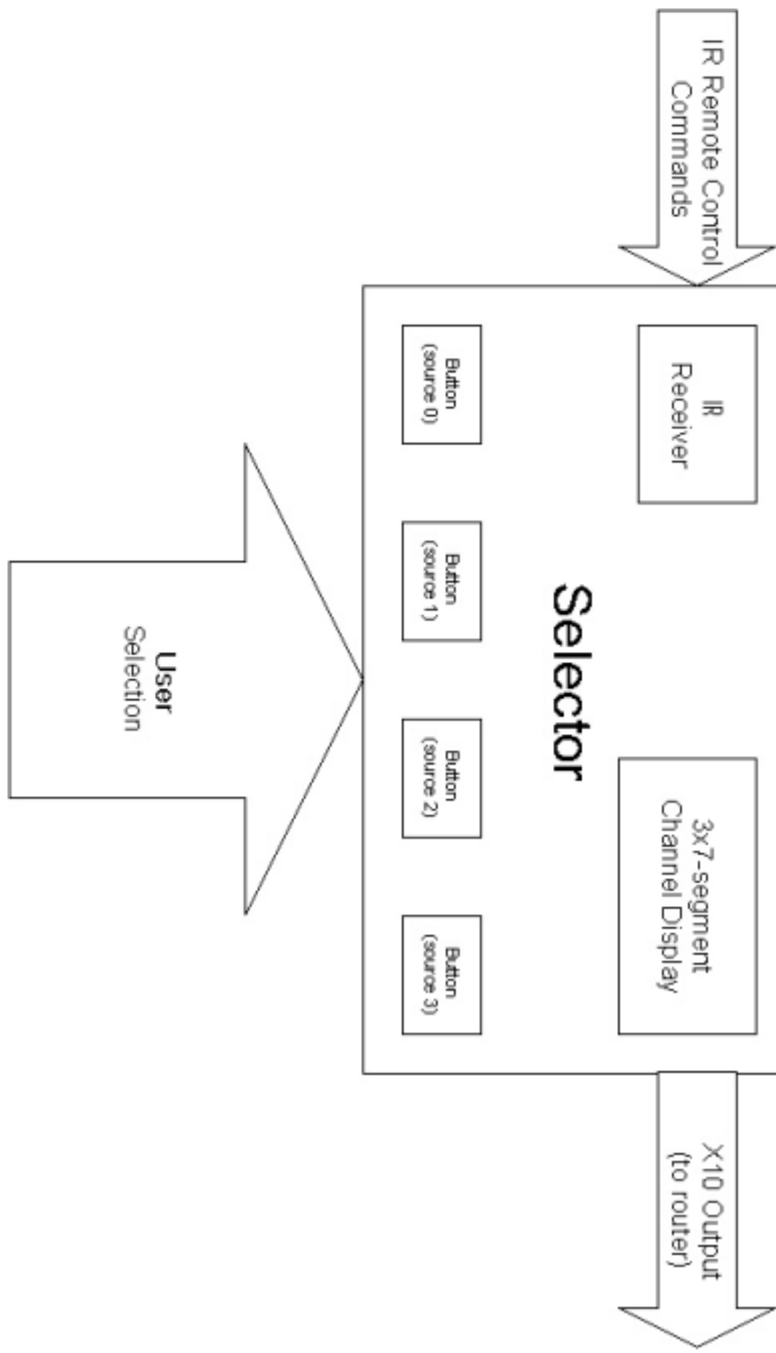

Figure 6:: Selector Block Diagram

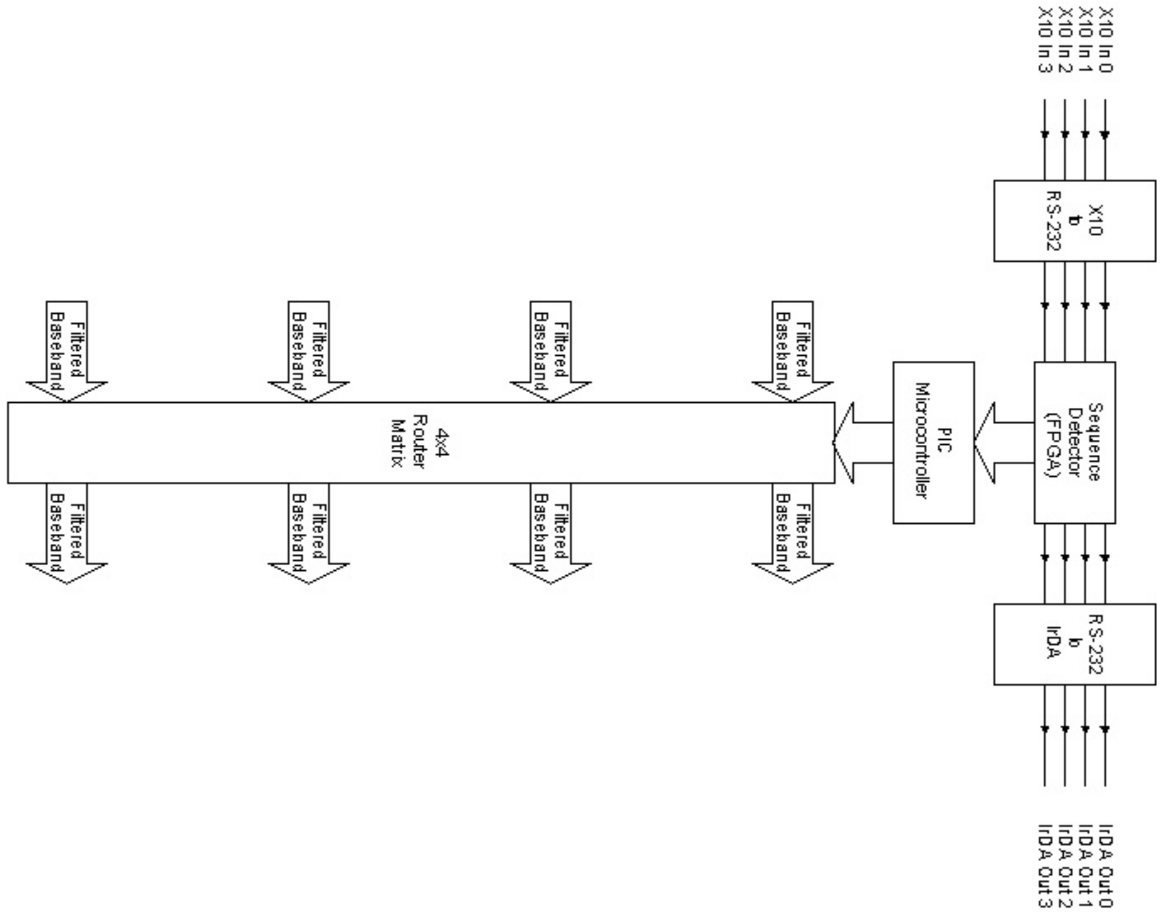

Figure 7:: Selector-to-Router Block Diagram

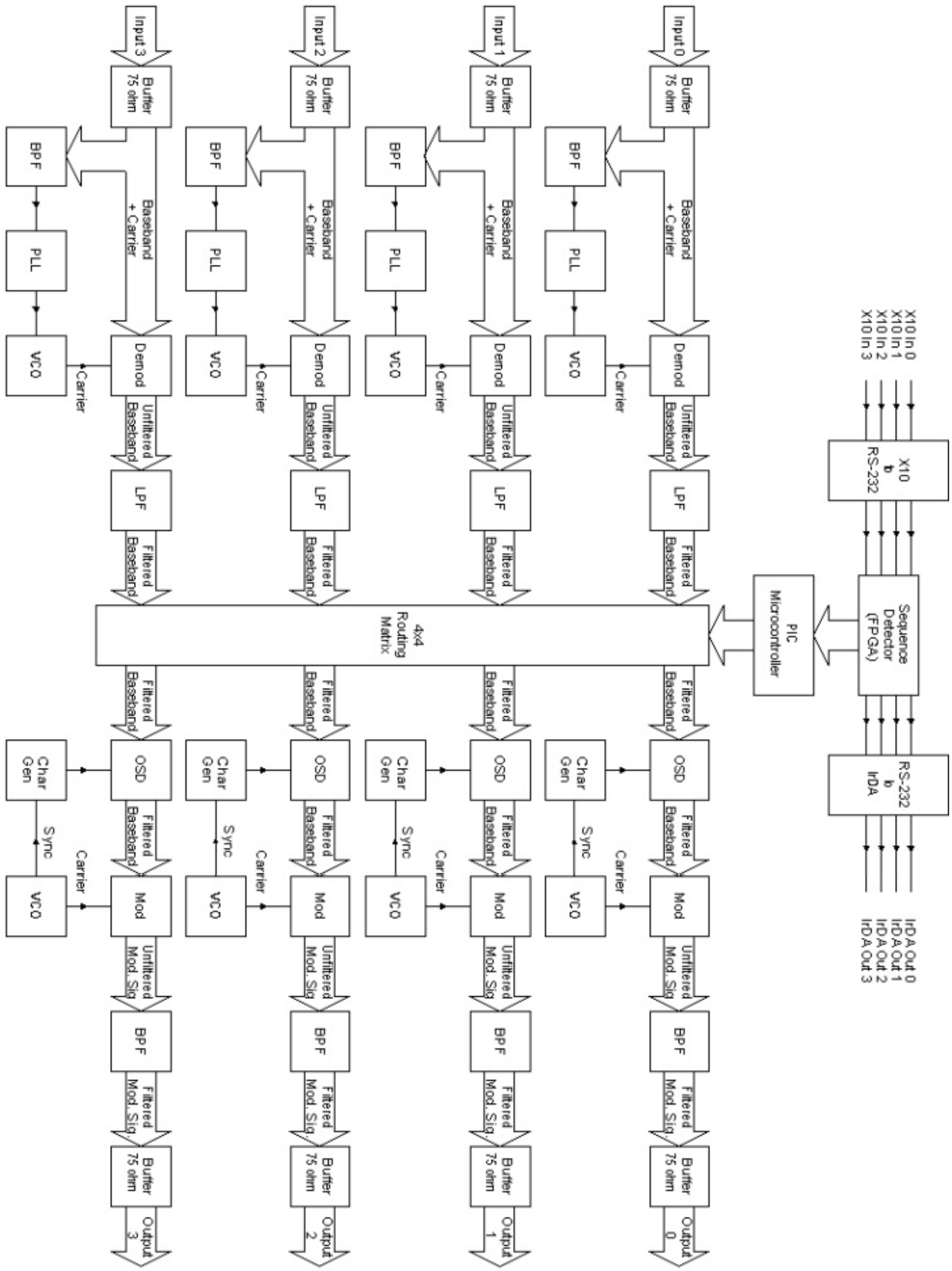

Figure 8:: System Block Diagram

5.2 Theory of Operation

Psonix's home video router (HVR-1000) is meant to enable users to watch one input in multiple locations or multiple outputs at different locations. The product has two basic components: a remote selector unit (selector), and a central video distribution unit (router). This section of the document outlines the basic operation of both components, and details the process in which signal is distributed from the central hub to the individual television stations.

5.2.1 Selector:

The purpose of this device is to forward standard remote control commands to the router, and to control the router for the purpose of video source selection. Information is sent to the router using in band, continuous frequency for signaling. A microcontroller arbitrates mastering over the link between remote control commands and router commands.

A continuous tone is always present to indicate the desired input router input. A FPGA is respsonsible for generating the tone to be sent over the coaxial cable for detection at the router. In reality, two separate tones are used – one for modulating the IR commands, and an always tone to indicate the input selection at the router.

Generation of the frequency is based on cycling a tabled index (as indicated in figure x). As the FPGA cycles through each entry in the lookup table, it decides what the next increment should be to generate the proper tone (1kHz, 2 kHz, 4 kHz, or 8 kHz).

The selector segment of the product is designed to allow the user to change inputs on the video distribution point, and relay IR commands between segments of the house utilizing the video router. The selector comprises the heart of the HVR, and its failure would cause the entire system to cease functioning. As previously noted, the selector also doubles as a development board, with added functionality.

The prominent feature of the selector will be the IR receiver, responsible for decoding the 38.5 KHz modulated IR data stream. The IR receiver consists of a phototransistor, a demodulator, and frequency filter to remove stray effects from ambient light. The output of the IR is remodulated on the separate control frequency generated by the FPGA.

5.2.2 Router:

The 4x4 router has 4 standard video inputs and 4 standard video outputs. The switching matrix is electronically-controlled, and independently feeds multiple video sources to multiple destinations. The overall router design is comprised of filters, switches, and buffers. The properly terminated inputs, and correct source impedances at the outputs provide a transparent video path for each input device. The video inputs accept NTSC video, plus audio modulated for channel 3 (carrier freq. at 61.25MHz, bandwidth 6.0 MHz).

At the input, the signal is fed through a lowpass filter to remove unwanted noise and any interference. The four input signals, after filtering, are passed into the router. Signal routing is accomplished by the enabling and disabling a four port analog mux. The routing matrix consists of two layers of op amps. The first layer contains a digitally controlled gain stage governed by ($A = 0$, or $A = -1$). The second layer consists of the summing op amps that act as signal buffers ($A = -1$).

The selector has a series of four frequency detectors at the output to allow for bi-directional information to be passed to the router. Each filter is a first order notch filter, with f_c centered at 1 kHz, 2 kHz, 4 kHz, and 8 kHz. As the tones are generated by the selector, the appropriate notch filter will allow the signal to pass. After passing through the notch filter, the signal output is passed through an op-amp to generate a nearly linear TTL output. To insure the proper voltage is sent however, and remove any extra ripple, the output is buffered, allowing for a +5/-5V signal.

This output (DC) voltage from the frequency detector is used to drive the analog mux to signify which output is to be sent to the selector on the coaxial cable.

5.3 Major Design Calculations

Major Design Calculations for this project were very simple. We knew that we wanted video inputs and video outputs, so bandwidth was immediately an issue. We had a very specific problem with bandwidth, namely, that we needed to reduce the bandwidth of our op amps by a generous margin to 160MHz.

$$f_c = 1/(2*pi*RC) = 160MHz$$

We chose an arbitrary resistor value of 75 ohms, and the equation produced a capacitor with value 10 pF.

We also knew that gain was going to be a specific need. Because we need an output consistent with our input, though, all the math involved reduces to unity gain. Each amp has negative unity gain, but two layers of amps causes it to be positive again:

$$A_g = -1*-1 = 1V/V$$

All other system calculations were per-case based filter calculations, using only resistors and capacitors, or voltage division calculations involving specifically matched resistors. Other calculations indirectly related to the system were cost calculations and labor-hour calculations used in dividing up the workload.

5.4 Schematic Layout

On the following sheets the reader will find the schematic layout for our project, including the router schematic, the detail single-signal path schematic, and the selector schematic. On the first schematic page is the linking schematic that shows the relationship between all the subsystem schematics.

These schematics have been heavily updated from the schematics we had last semester. During the course of our design, we found it easier to place schematics in PROTEL since we were planning on using them there anyway to design our PCBs from. The schematics you see in the following pages are all PROTEL schematics, and may appear a little grainy when you look at them. This surprising low detail can be remedied if you have PROTEL at your disposal. In the senior project disk, we have included the files for both schematic AND PCB, so that the reader can have a better look at the design of our project.

Please note that for a closer look at each schematic, you can open the file on the CD attached with this report.

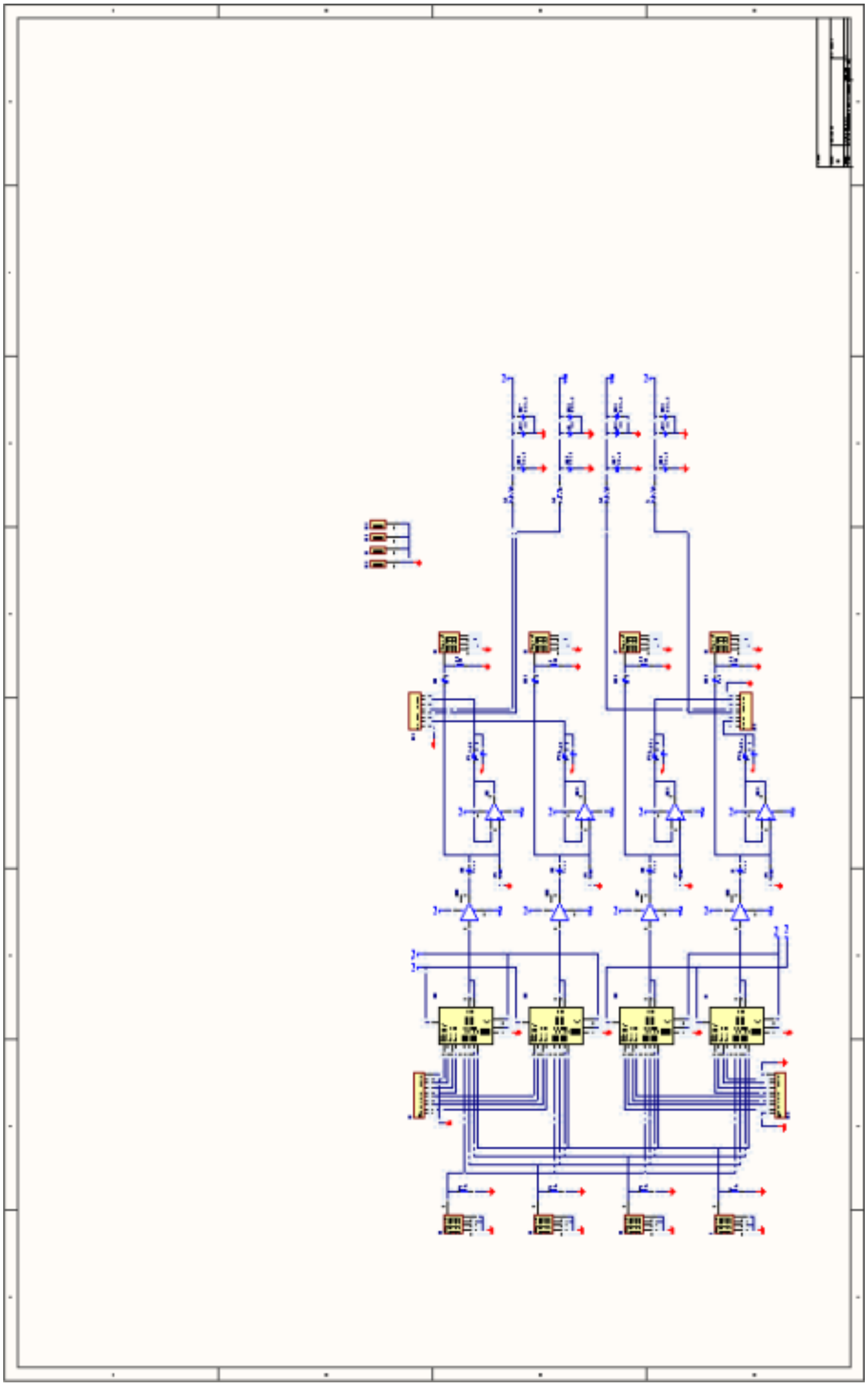

Figure 9:: HVR-1000 Router Board Schematic

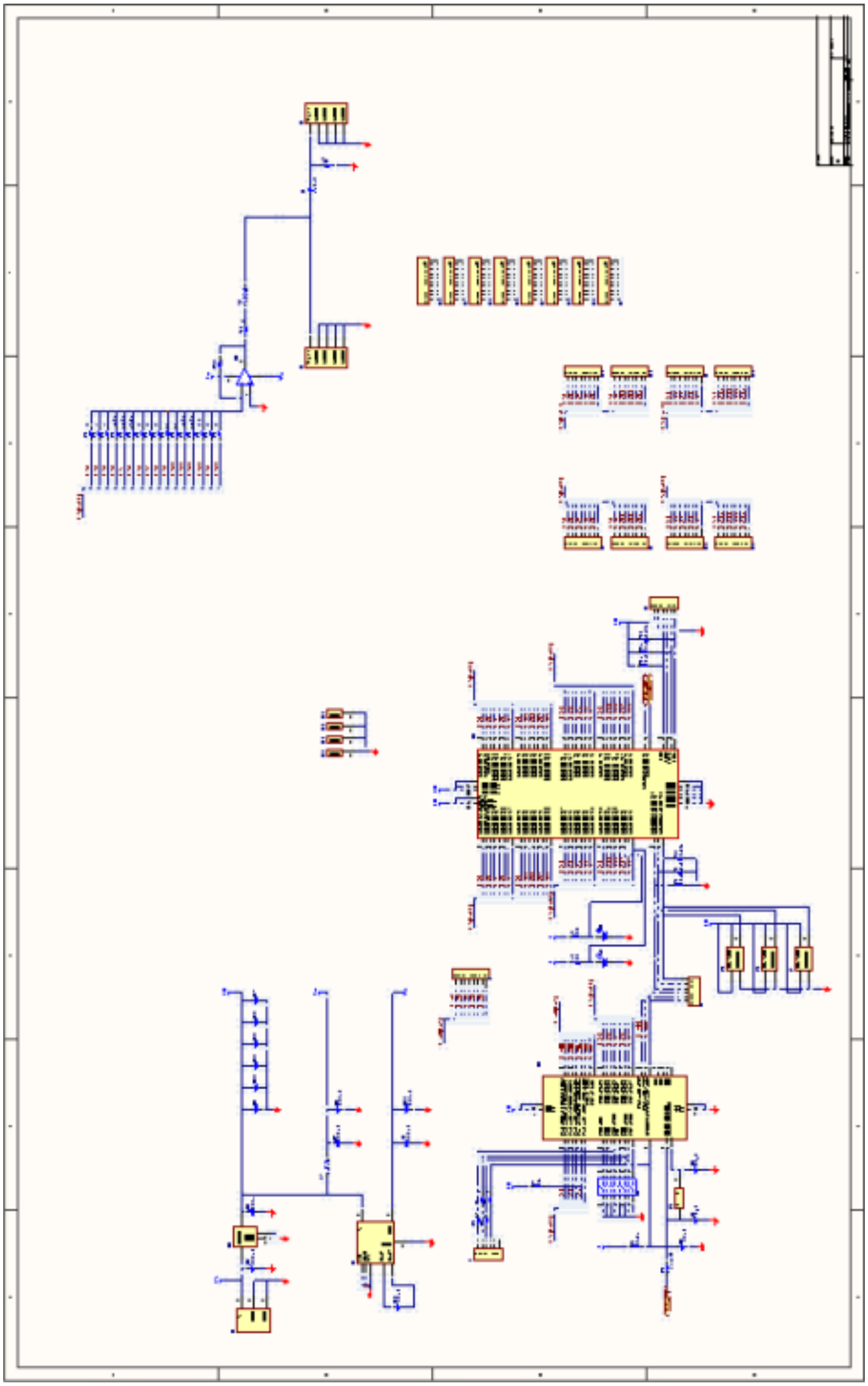

Figure 10:: HVR-1000 Selector Board Scematic

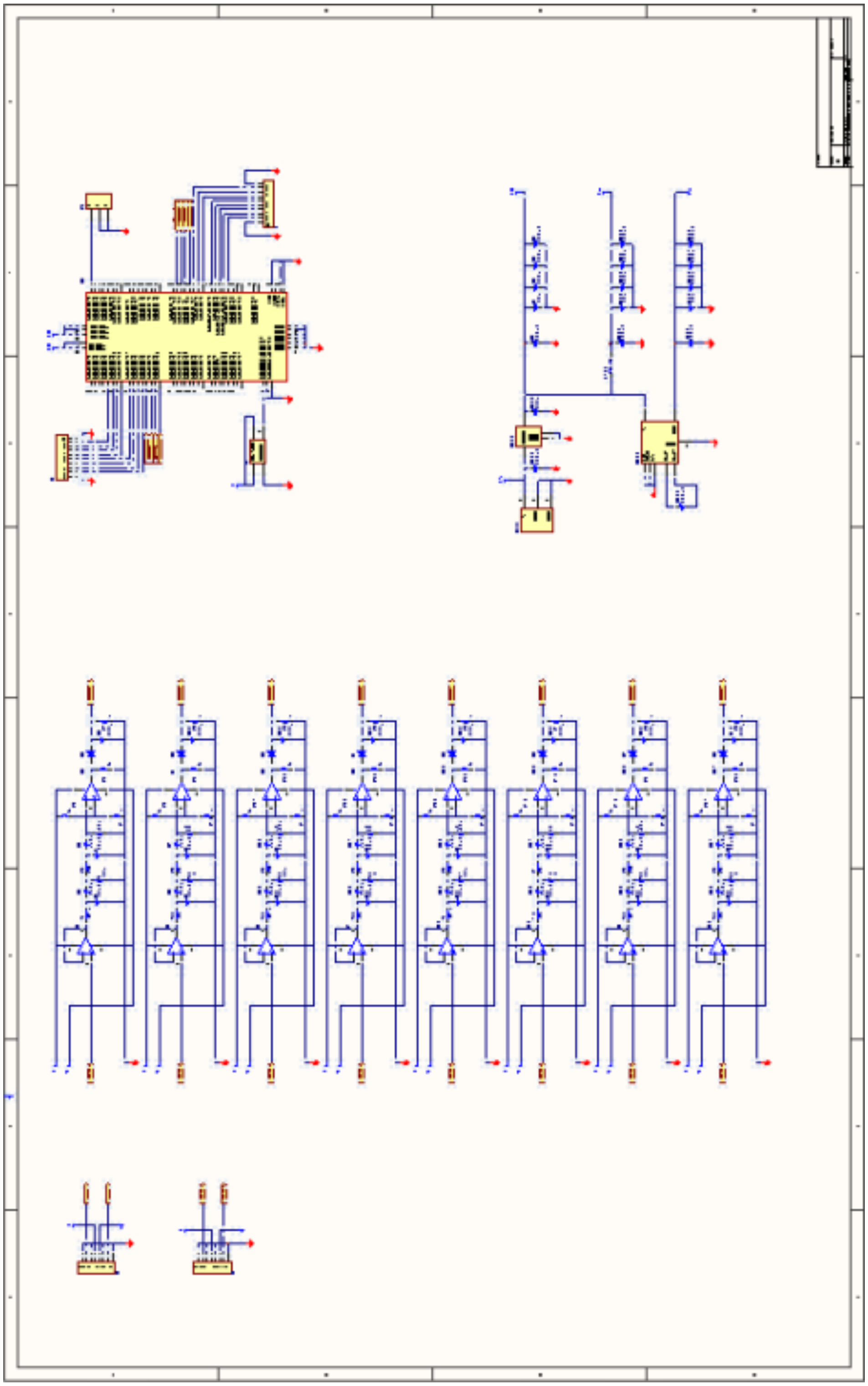

Figure 11:: HVR-1000 Controller Board Schematic

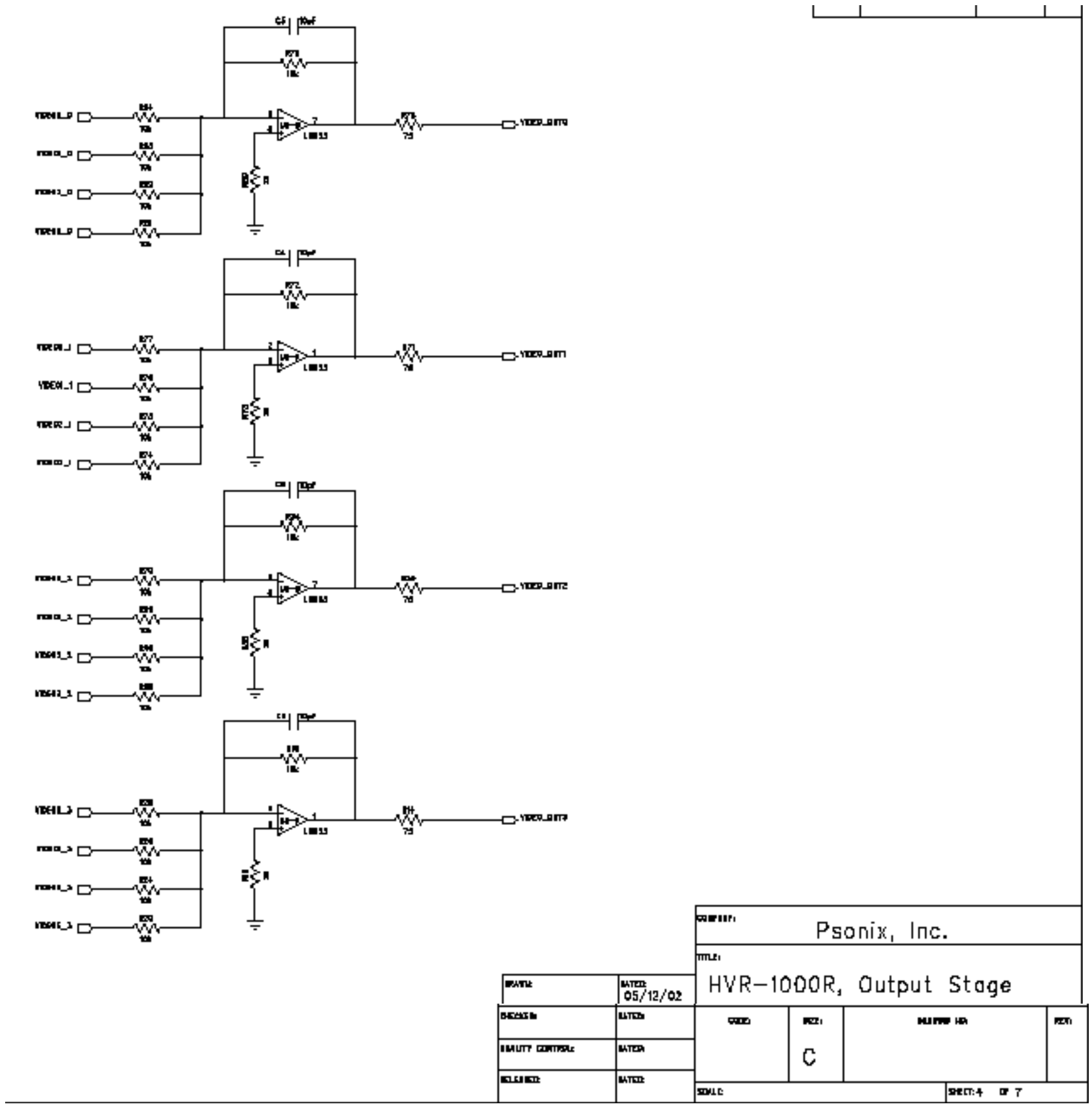

Figure 12:: HVR-1000R Output Stage

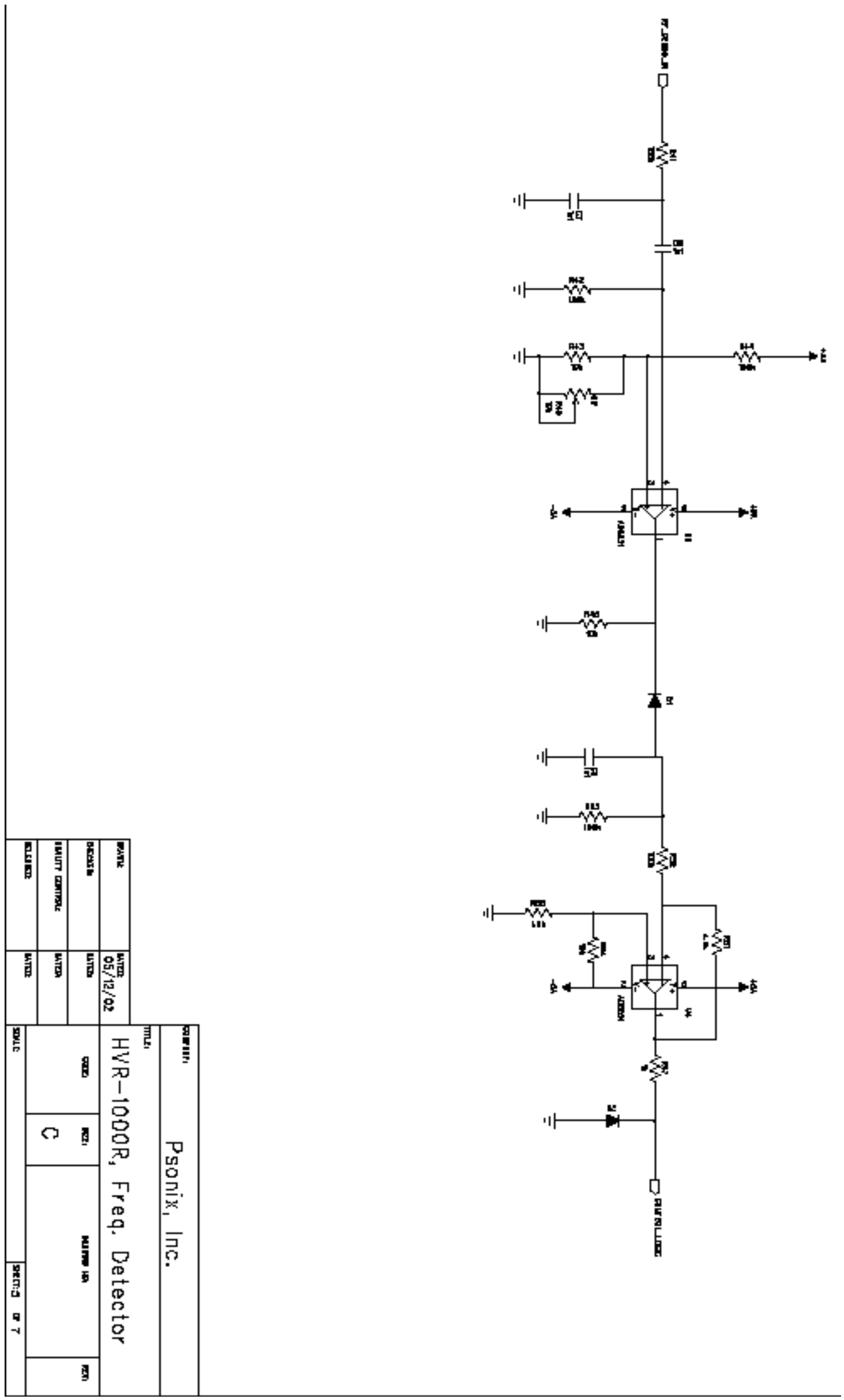

Figure 13:: HVR-1000R Frequency Detector

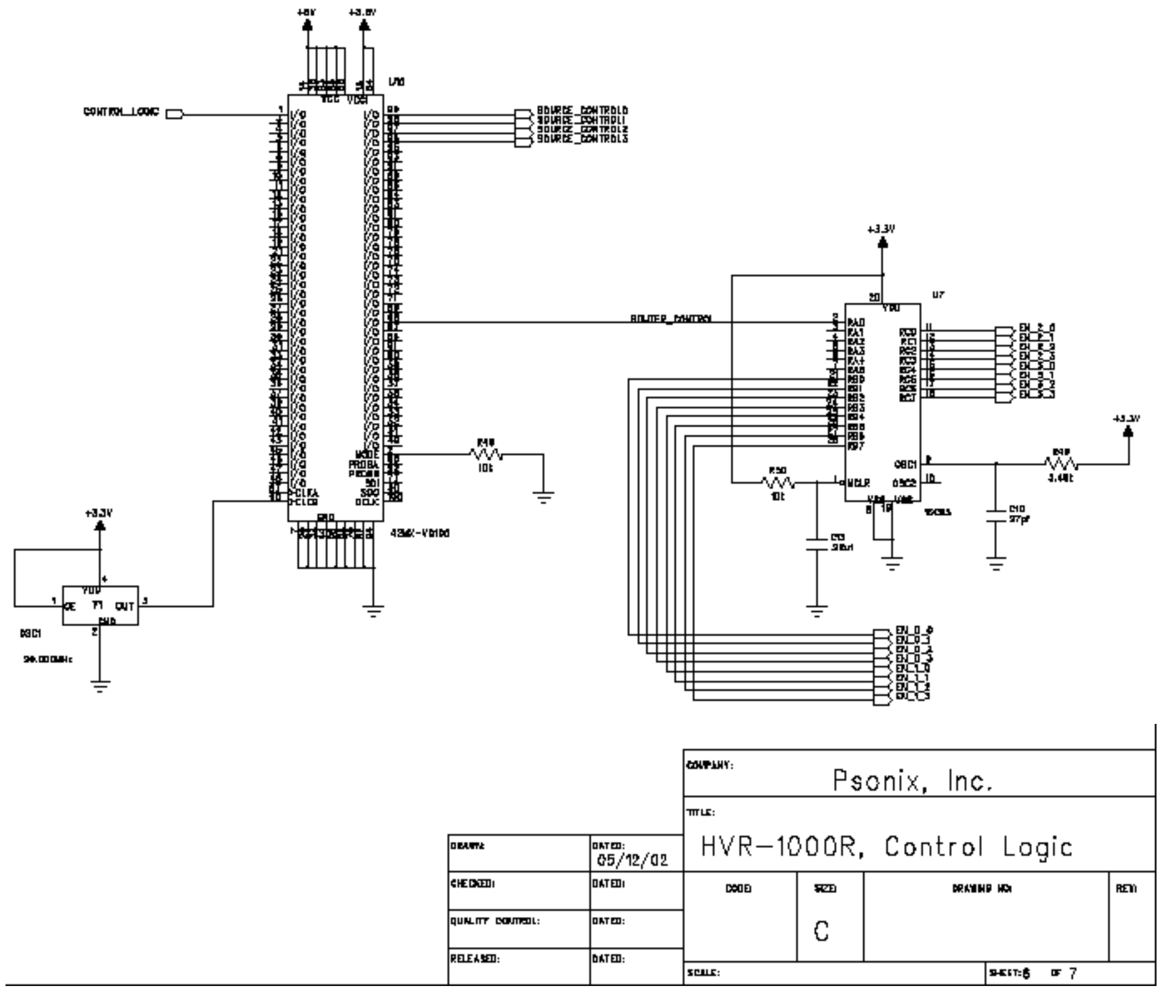

Figure 14:: HVR-1000R Control Logic

5.5 Parts List

Following are the parts lists generated from our schematics. Some adjustments were made, and not all of the parts listed are on our physical board, although they are all listed here. This parts list generally incorporates everything we used and thought we were going to need for the finished product. It includes all units required to create the exact system outlined in the schematics above.

There is one parts list for the router board, one parts list for the selector board, and one parts list for the controller board.

5.5.1 Router Parts List

Designator	Value	Description	Footprint
J1			BU_BNC10X10H
J10		Header, 10-Pin	HDR1X10
J11		Header, 8-Pin	HDR1X8
J12		Header, 8-Pin	HDR1X8
J13			440hole
J14			440hole
J15			440hole
J16			440hole
J2			BU_BNC10X10H
J3			BU_BNC10X10H
J4			BU_BNC10X10H
J5			BU_BNC10X10H
J6			BU_BNC10X10H
J7			BU_BNC10X10H
J8			BU_BNC10X10H
J9		Header, 10-Pin	HDR1X10
U1		Analog Mux, -3dB @ 750MHz	DIP-14
U10		Low Cost, High-Speed Rail-to-Rail Amplifier	SO-G5/P.95
U11		Low Cost, High-Speed Rail-to-Rail Amplifier	SO-G5/P.95
U12		Low Cost, High-Speed Rail-to-Rail Amplifier	SO-G5/P.95
U2		Analog Mux, -3dB @ 750MHz	DIP-14
U3		Analog Mux, -3dB @ 750MHz	DIP-14
U4		Analog Mux, -3dB @ 750MHz	DIP-14
U5		Low Cost, High-Speed Rail-to-Rail Amplifier	SO-G5/P.95
U6		Low Cost, High-Speed Rail-to-Rail Amplifier	SO-G5/P.95
U7		Low Cost, High-Speed Rail-to-Rail Amplifier	SO-G5/P.95
U8		Low Cost, High-Speed Rail-to-Rail Amplifier	SO-G5/P.95
U9		Low Cost, High-Speed Rail-to-Rail Amplifier	SO-G5/P.95
R10	1.58k	Resistor	CC2012-0805
R11	1.58k	Resistor	CC2012-0805
R12	1.58k	Resistor	CC2012-0805
R9	1.58k	Resistor	CC2012-0805
C13	100nF	Capacitor	CC2012-0805
C14	100nF	Capacitor	CC2012-0805
C15	100nF	Capacitor	CC2012-0805
C16	100nF	Capacitor	CC2012-0805

C17	100nF	Capacitor	CC2012-0805
C18	100nF	Capacitor	CC2012-0805
C19	100nF	Capacitor	CC2012-0805
C20	100nF	Capacitor	CC2012-0805
C1	10nF	Capacitor	CC2012-0805
C2	10nF	Capacitor	CC2012-0805
C3	10nF	Capacitor	CC2012-0805
C4	10nF	Capacitor	CC2012-0805
C25	10uF	Polarized Capacitor (Surface Mount)	C3216-1206
C26	10uF	Polarized Capacitor (Surface Mount)	C3216-1206
C27	10uF	Polarized Capacitor (Surface Mount)	C3216-1206
C28	10uF	Polarized Capacitor (Surface Mount)	C3216-1206
R1	1K	Resistor	CC2012-0805
R2	1K	Resistor	CC2012-0805
R3	1K	Resistor	CC2012-0805
R4	1K	Resistor	CC2012-0805
R13	1M	Resistor	CC2012-0805
R14	1M	Resistor	CC2012-0805
R15	1M	Resistor	CC2012-0805
R16	1M	Resistor	CC2012-0805
R5	1M	Resistor	CC2012-0805
R6	1M	Resistor	CC2012-0805
R7	1M	Resistor	CC2012-0805
R8	1M	Resistor	CC2012-0805
C5	1nF	Capacitor	CC2012-0805
C6	1nF	Capacitor	CC2012-0805
C7	1nF	Capacitor	CC2012-0805
C8	1nF	Capacitor	CC2012-0805
C10	1uF	Capacitor	CC2012-0805
C11	1uF	Capacitor	CC2012-0805
C12	1uF	Capacitor	CC2012-0805
C9	1uF	Capacitor	CC2012-0805
L1	5.6uH	Inductor	C3225-1210
L2	5.6uH	Inductor	C3225-1210
L3	5.6uH	Inductor	C3225-1210
L4	5.6uH	Inductor	C3225-1210

5.5.2 Selector Parts List

Designator	Value	Description	Footprint
C10		Capacitor	cc2012-0805
C11		Capacitor	cc2012-0805
C12		Capacitor	cc2012-0805
C16		Capacitor	cc2012-0805
C17		Capacitor	cc2012-0805
C8		Capacitor	cc2012-0805
D1		Photosensitive Diode	PIN2
J1			Kat
J10		Header, 8-Pin	HDR1X8
J11		Header, 8-Pin	HDR1X8

J12		Header, 8-Pin	HDR1X8
J13		Header, 8-Pin	HDR1X8
J14		Header, 8-Pin	HDR1X8
J15		Header, 8-Pin	HDR1X8
J16		Header, 10-Pin	HDR1X10
J17		Header, 10-Pin	HDR1X10
J18		Header, 10-Pin	HDR1X10
J19		Header, 10-Pin	HDR1X10
J2			F-Connector_1
J20			PCBComponent_1
J21			PCBComponent_1
J22			PCBComponent_1
J23			PCBComponent_1
J24		Header, 10-Pin	HDR1X10
J25		Header, 10-Pin	HDR1X10
J26		Header, 10-Pin	HDR1X10
J27		Header, 10-Pin	HDR1X10
J3			F-Connector_1
J4		Header, 6-Pin	HDR1X6
J5		Header, 6-Pin	HDR1X6
J6		Header, 6-Pin	HDR1X6
J7		Header, 8-Pin	HDR1X8
J8		Header, 8-Pin	HDR1X8
J9		Header, 8-Pin	HDR1X8
S1		DIP Switch	DIP-16
S2		Photosensitive Diode	PIN2
U1		EPROM-Based 8-Bit CMOS Microcontroller	QFP10x10-G44/G10N
U2		Programmable CPLD	QCC-J84/Y1.8
U3		Low Cost, High-Speed Rail-to-Rail Amplifier	SO-G5/P.95
U4			SOP8
U5			3 Lead TO-263 (U)
Y1			HCM49
Y2			CMX-750P
Y3			CMX-750P
Y4			CMX-750P
R1	0	Resistor	CC2012-0805
R10	10.0K	Resistor	CC2012-0805
R11	10.0K	Resistor	CC2012-0805
R12	10.0K	Resistor	CC2012-0805
R13	10.0K	Resistor	CC2012-0805
R2	10.0k	Resistor	CC2012-0805
R8	10.0K	Resistor	CC2012-0805
R9	10.0K	Resistor	CC2012-0805
C1	100nF	Capacitor	cc2012-0805
C15	100nF	Capacitor	cc2012-0805
C4	100nF	Capacitor	cc2012-0805
C9	100nF	Capacitor	cc2012-0805
C13	100uF	Polarized Capacitor (Surface Mount)	C3216-1206

C14	100uF	Polarized Capacitor (Surface Mount)	C3216-1206
C5	100uF	Polarized Capacitor (Surface Mount)	C3216-1206
C6	100uF	Polarized Capacitor (Surface Mount)	C3216-1206
C7	100uF	Polarized Capacitor (Surface Mount)	C3216-1206
L1	100uH	Inductor	C3225-1210
R19	16.2k	Resistor	CC2012-0805
R27	16.2k	Resistor	CC2012-0805
C2	18pF	Capacitor	cc2012-0805
C3	18pF	Capacitor	cc2012-0805
R15	1k	Resistor	CC2012-0805
R23	1k	Resistor	CC2012-0805
R3	1k	Resistor	CC2012-0805
R4	1k	Resistor	CC2012-0805
R5	1k	Resistor	CC2012-0805
R6	1k	Resistor	CC2012-0805
R7	1K	Resistor	CC2012-0805
R32	1M	Resistor	CC2012-0805
R16	2k	Resistor	CC2012-0805
R24	2k	Resistor	CC2012-0805
R20	32.4k	Resistor	CC2012-0805
R28	32.4k	Resistor	CC2012-0805
R33	330	Resistor	CC2012-0805
R34	330	Resistor	CC2012-0805
R17	4.02k	Resistor	CC2012-0805
R25	4.02k	Resistor	CC2012-0805
R14	499	Resistor	CC2012-0805
R22	499	Resistor	CC2012-0805
R30	499	Resistor	CC2012-0805
L2	5.6uH	Inductor	C3225-1210
R21	63.4k	Resistor	CC2012-0805
R29	63.4k	Resistor	CC2012-0805
R31	75	Resistor	CC2012-0805
R18	8.06k	Resistor	CC2012-0805
R26	8.06k	Resistor	CC2012-0805

5.5.3 Controller Parts List

Designator	Value	Description	Footprint
D1		Default Diode	SO-G3/Z3.3
D2		Default Diode	SO-G3/Z3.3
D3		Default Diode	SO-G3/Z3.3
D4		Default Diode	SO-G3/Z3.3
D5		Default Diode	SO-G3/Z3.3
D6		Default Diode	SO-G3/Z3.3
D7		Default Diode	SO-G3/Z3.3
D8		Default Diode	SO-G3/Z3.3
J?			CMX-750P
J1		Header, 8-Pin	HDR1X8
J100			Kat
J2		Header, 10-Pin	HDR1X10

J3		Header, 8-Pin	HDR1X8
J4		Header, 10-Pin	HDR1X10
P1			3.5 Jack
U1		Low Cost, High-Speed Rail-to-Rail Amplifier	SO-G5/P.95
U10		Low Cost, High-Speed Rail-to-Rail Amplifier	SO-G5/P.95
U100			3 Lead TO-263 (U)
U101			SOP8
U11		Low Cost, High-Speed Rail-to-Rail Amplifier	SO-G5/P.95
U12		Low Cost, High-Speed Rail-to-Rail Amplifier	SO-G5/P.95
U13		Low Cost, High-Speed Rail-to-Rail Amplifier	SO-G5/P.95
U14		Low Cost, High-Speed Rail-to-Rail Amplifier	SO-G5/P.95
U15		Low Cost, High-Speed Rail-to-Rail Amplifier	SO-G5/P.95
U16		Low Cost, High-Speed Rail-to-Rail Amplifier	SO-G5/P.95
U17		Low Cost, High-Speed Rail-to-Rail Amplifier	SO-G5/P.95
U2		Low Cost, High-Speed Rail-to-Rail Amplifier	SO-G5/P.95
U3		Low Cost, High-Speed Rail-to-Rail Amplifier	SO-G5/P.95
U4		Low Cost, High-Speed Rail-to-Rail Amplifier	SO-G5/P.95
U5		Low Cost, High-Speed Rail-to-Rail Amplifier	SO-G5/P.95
U6		Low Cost, High-Speed Rail-to-Rail Amplifier	SO-G5/P.95
U7		Low Cost, High-Speed Rail-to-Rail Amplifier	SO-G5/P.95
U8		Low Cost, High-Speed Rail-to-Rail Amplifier	SO-G5/P.95
U9		Programmable CPLD	QCC-J84/Y1.8
R18	1.58k	Resistor	CC2012-0805
R19	1.58k	Resistor	CC2012-0805
R2	1.58k	Resistor	CC2012-0805
R20	1.58k	Resistor	CC2012-0805
R21	1.58k	Resistor	CC2012-0805
R3	1.58k	Resistor	CC2012-0805
R34	1.58k	Resistor	CC2012-0805
R35	1.58k	Resistor	CC2012-0805
R36	1.58k	Resistor	CC2012-0805
R37	1.58k	Resistor	CC2012-0805
R4	1.58k	Resistor	CC2012-0805
R5	1.58k	Resistor	CC2012-0805
R50	1.58k	Resistor	CC2012-0805
R51	1.58k	Resistor	CC2012-0805
R52	1.58k	Resistor	CC2012-0805
R53	1.58k	Resistor	CC2012-0805
R10	100	Resistor	CC2012-0805
R11	100	Resistor	CC2012-0805
R12	100	Resistor	CC2012-0805
R13	100	Resistor	CC2012-0805
R26	100	Resistor	CC2012-0805
R27	100	Resistor	CC2012-0805
R28	100	Resistor	CC2012-0805
R29	100	Resistor	CC2012-0805
R42	100	Resistor	CC2012-0805
R43	100	Resistor	CC2012-0805

R44	100	Resistor	CC2012-0805
R45	100	Resistor	CC2012-0805
R58	100	Resistor	CC2012-0805
R59	100	Resistor	CC2012-0805
R60	100	Resistor	CC2012-0805
R61	100	Resistor	CC2012-0805
C?	100nF	Capacitor	CC2012-0805
C?	100nF	Capacitor	CC2012-0805
C?	100nF	Capacitor	CC2012-0805
C1	100nF	Capacitor	CC2012-0805
C103	100nF	Capacitor	CC2012-0805
C104	100nF	Capacitor	CC2012-0805
C105	100nF	Capacitor	CC2012-0805
C106	100nF	Capacitor	CC2012-0805
C107	100nF	Capacitor	CC2012-0805
C108	100nF	Capacitor	CC2012-0805
C11	100nF	Capacitor	CC2012-0805
C110	100nF	Capacitor	CC2012-0805
C112	100nF	Capacitor	CC2012-0805
C12	100nF	Capacitor	CC2012-0805
C13	100nF	Capacitor	CC2012-0805
C14	100nF	Capacitor	CC2012-0805
C16	100nF	Capacitor	CC2012-0805
C17	100nF	Capacitor	CC2012-0805
C18	100nF	Capacitor	CC2012-0805
C19	100nF	Capacitor	CC2012-0805
C2	100nF	Capacitor	CC2012-0805
C21	100nF	Capacitor	CC2012-0805
C22	100nF	Capacitor	CC2012-0805
C23	100nF	Capacitor	CC2012-0805
C24	100nF	Capacitor	CC2012-0805
C26	100nF	Capacitor	CC2012-0805
C27	100nF	Capacitor	CC2012-0805
C28	100nF	Capacitor	CC2012-0805
C29	100nF	Capacitor	CC2012-0805
C3	100nF	Capacitor	CC2012-0805
C31	100nF	Capacitor	CC2012-0805
C32	100nF	Capacitor	CC2012-0805
C33	100nF	Capacitor	CC2012-0805
C34	100nF	Capacitor	CC2012-0805
C36	100nF	Capacitor	CC2012-0805
C37	100nF	Capacitor	CC2012-0805
C38	100nF	Capacitor	CC2012-0805
C39	100nF	Capacitor	CC2012-0805
C4	100nF	Capacitor	CC2012-0805
C6	100nF	Capacitor	CC2012-0805
C7	100nF	Capacitor	CC2012-0805
C8	100nF	Capacitor	CC2012-0805

C9	100nF	Capacitor	CC2012-0805
C10	100pF	Capacitor	CC2012-0805
C15	100pF	Capacitor	CC2012-0805
C20	100pF	Capacitor	CC2012-0805
C25	100pF	Capacitor	CC2012-0805
C30	100pF	Capacitor	CC2012-0805
C35	100pF	Capacitor	CC2012-0805
C40	100pF	Capacitor	CC2012-0805
C5	100pF	Capacitor	CC2012-0805
C?	100uF	Polarized Capacitor (Surface Mount)	C3216-1206
C100	100uF	Polarized Capacitor (Surface Mount)	C3216-1206
C101	100uF	Polarized Capacitor (Surface Mount)	C3216-1206
C102	100uF	Polarized Capacitor (Surface Mount)	C3216-1206
C109	100uF	Polarized Capacitor (Surface Mount)	C3216-1206
C111	100uF	Polarized Capacitor (Surface Mount)	C3216-1206
R1	1K	Resistor	CC2012-0805
R14	1K	Resistor	CC2012-0805
R15	1K	Resistor	CC2012-0805
R16	1K	Resistor	CC2012-0805
R17	1K	Resistor	CC2012-0805
R22	1K	Resistor	CC2012-0805
R23	1K	Resistor	CC2012-0805
R24	1K	Resistor	CC2012-0805
R25	1K	Resistor	CC2012-0805
R30	1K	Resistor	CC2012-0805
R31	1K	Resistor	CC2012-0805
R32	1K	Resistor	CC2012-0805
R33	1K	Resistor	CC2012-0805
R38	1K	Resistor	CC2012-0805
R39	1K	Resistor	CC2012-0805
R40	1K	Resistor	CC2012-0805
R41	1K	Resistor	CC2012-0805
R46	1K	Resistor	CC2012-0805
R47	1K	Resistor	CC2012-0805
R48	1K	Resistor	CC2012-0805
R49	1K	Resistor	CC2012-0805
R54	1K	Resistor	CC2012-0805
R55	1K	Resistor	CC2012-0805
R56	1K	Resistor	CC2012-0805
R57	1K	Resistor	CC2012-0805
R6	1K	Resistor	CC2012-0805
R62	1K	Resistor	CC2012-0805
R63	1K	Resistor	CC2012-0805
R64	1K	Resistor	CC2012-0805
R7	1K	Resistor	CC2012-0805
R8	1K	Resistor	CC2012-0805
R9	1K	Resistor	CC2012-0805
L100	5.6uH	Inductor	C3225-1210

5.6 Wire List

Following is a wire list for the system. A wire list details which connections go to where, and shows in written form the connections that link which inputs to which outputs. The wire list is a method of tracking the system and may be useful later in troubleshooting and system analysis.

This wire list is also known as a net list. It is used to explain the links between all separate parts of the system. While not pretty to look at, it can be used in the program from which it came to perform analysis on a system and track down alterations that may be somehow causing problems. The net list is very useful in PSPICE, especially when trying to track down a particular node or lose end that is causing a problem when you simulate. The following is the net list from the same system as the parts list above, so part names should correlate between lists.

Once again, there is a wire list for each of the three boards that we created for this project; a wire list for the selector, a wire list for the router, and a wire list for the controller.

5.6.1 Router Wire List

(NetC9_2	C9-2	J5-1	R13-2)	
(NetC10_2	C10-2	J6-1	R14-2)	
(NetC11_2	C11-2	J7-1	R15-2)	
(NetC12_2	C12-2	J8-1	R16-2)	
(NetJ11_4	J11-4	L1-1)		
(NetJ12_5	J12-5	L3-1)		
(NetJ11_5	J11-5	L2-1)		
(NetJ12_4	J12-4	L4-1)		
(NetC7_2	C7-2	J12-7	R11-1)	
(NetC5_2	C5-2	J11-2	R9-1)	
(NetC6_2	C6-2	J11-7	R10-1)	
(NetC8_2	C8-2	J12-2	R12-1)	
(NetR12_2	R12-2	U12-1	U12-4)	
(NetR11_2	R11-2	U11-1	U11-4)	
(NetR10_2	R10-2	U10-1	U10-4)	
(NetR9_2	R9-2	U9-1	U9-4)	
(NetC4_2	C4-2	C12-1	R8-1	U12-3)
(NetC3_2	C3-2	C11-1	R7-1	U11-3)
(NetC2_2	C2-2	C10-1	R6-1	U10-3)
(NetC1_2	C1-2	C9-1	R5-1	U9-3)
(NetC4_1	C4-1	U8-5)		
(NetC3_1	C3-1	U7-5)		
(NetC2_1	C2-1	U6-5)		

(NetC1_1 C1-1 U5-5)
(NetU1_10 U1-10 U1-12 U5-3)
(NetU4_10 U4-10 U4-12 U8-3)
(NetU2_10 U2-10 U2-12 U6-3)
(NetJ9_2 J9-2 U1-14)
(NetJ10_2 J10-2 U4-9)
(NetJ9_3 J9-3 U1-8)
(NetJ10_3 J10-3 U4-13)
(NetJ9_4 J9-4 U1-13)
(NetJ10_4 J10-4 U4-8)
(NetJ9_5 J9-5 U1-9)
(NetJ10_5 J10-5 U4-14)
(NetJ9_6 J9-6 U2-14)
(NetJ10_6 J10-6 U3-9)
(NetJ9_7 J9-7 U2-8)
(NetJ10_7 J10-7 U3-13)
(NetJ9_8 J9-8 U2-13)
(NetJ10_8 J10-8 U3-8)
(NetJ9_9 J9-9 U2-9)
(NetJ10_9 J10-9 U3-14)
(NetJ4_1 J4-1 R4-2 U1-7 U2-7 U3-7 U4-7)
(NetJ2_1 J2-1 R2-2 U1-3 U2-3 U3-3 U4-3)
(NetJ3_1 J3-1 R3-2 U1-5 U2-5 U3-5 U4-5)
(NetJ1_1 J1-1 R1-2 U1-1 U2-1 U3-1 U4-1)
(GND C5-1 C6-1 C7-1 C8-1 C13-1 C14-1 C15-1 C16-1 C17-1
C18-1 C19-1 C20-1 C25-2 C26-2 C27-2 C28-2 J1-2 J1-3 J1-4
J1-5 J2-2 J2-3 J2-4 J2-5 J3-2 J3-3 J3-4 J3-5 J4-2
J4-3 J4-4 J4-5 J5-2 J5-3 J5-4 J5-5 J6-2 J6-3 J6-4
J6-5 J7-2 J7-3 J7-4 J7-5 J8-2 J8-3 J8-4 J8-5 J9-1
J9-10 J10-1 J10-10 J11-1 J11-3 J11-6 J11-8 J12-1 J12-3 J12-6
J12-8 J13-1 J14-1 J15-1 J16-1 R1-1 R2-1 R3-1 R4-1 R5-2
R6-2 R7-2 R8-2 R13-1 R14-1 R15-1 R16-1 U1-2 U1-6 U2-2
U2-6 U3-2 U3-6 U4-2 U4-6)
(-5A2 C15-2 C19-2 C27-1 L3-2 U3-11 U4-11 U7-2 U8-2 U11-2 U12-2)
(-5A1 C14-2 C18-2 C26-1 L2-2 U1-11 U2-11 U5-2 U6-2 U9-2 U10-2)

(+5A2 C16-2 C20-2 C28-1 L4-2 U3-4 U4-4 U7-4 U8-4 U11-5 U12-5)

(+5A1 C13-2 C17-2 C25-1 L1-2 U1-4 U2-4 U5-4 U6-4 U9-5 U10-5)

5.6.2 Selector Wire List

(PORTE2 J5-3 U1-27)

(PORTE1 J5-2 U1-26)

(PORTE0 J5-1 U1-25)

(PORTC7 J7-8 U1-1)

(PORTC6 J7-7 U1-44)

(PORTC5 J7-6 U1-43)

(PORTC4 J7-5 U1-42)

(PORTC3 J7-4 U1-37)

(PORTC2 J7-3 U1-36)

(PORTC1 J7-2 U1-35)

(PORTC0 J7-1 U1-32)

(NetR1_2 R1-2 U2-74)

(NetC4_1 C4-1 J3-1 R32-1)

(NetL1_1 L1-1 R31-1)

(NetC4_2 C4-2 J2-1 L1-2)

(NetR30_1 R30-1 R31-2 U3-1)

(NetR14_1 R14-1 R15-1 R16-1 R17-1 R18-1 R19-1 R20-1 R21-1
R22-1 R23-1 R24-1 R25-1 R26-1 R27-1 R28-1 R29-1 R30-2 U3-4)

(NetJ6_4 J6-4 U2-59)

(NetJ6_6 J6-6 R13-1 U2-30)

(NetJ6_5 J6-5 R12-1 U2-29)

(NetJ6_3 J6-3 R11-1 U2-28)

(NetJ5_6 J5-6 R10-2 U2-12 Y4-3)

(NetJ5_5 J5-5 R9-2 U2-10 Y3-3)

(NetJ5_4 J5-4 R8-2 U2-9 Y2-3)

(NetS1_11 S1-11 U1-15)

(NetS1_12 S1-12 U1-14)

(NetS1_14 S1-14 U1-10)

(NetS1_15 S1-15 U1-9)

(NetS1_16 S1-16 U1-8)

(NetC3_2 C3-2 U1-31 Y1-2)

(NetR4_1 R4-1 S1-10 U1-16)

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(NetR3_1   R3-1    S1-13   U1-11)
(NetR5_1   R5-1    S1-9    U1-17)
(NetJ4_4   J4-4    R6-2)
(NetJ4_3   J4-3    R5-2)
(NetJ4_2   J4-2    R4-2)
(NetJ4_1   J4-1    R3-2)
(NetC1_2   C1-2    R2-1    R6-1    U1-18)
(NetC2_2   C2-2    R1-1    U1-30   Y1-1)
(NetC13_2  C13-2   U4-4)
(NetC13_1  C13-1   U4-2)
(GPD15     J15-8   U2-72)
(GPD14     J15-7   U2-71)
(GPD13     J15-6   U1-24   U2-70)
(GPD12     J15-5   R7-1    U1-23   U2-69)
(GPD11     J15-4   U1-22   U2-68)
(GPD10     J15-3   U1-21   U2-67)
(GPD9  J15-2   U1-20   U2-66)
(GPD8  J15-1   U1-19   U2-65)
(GPD7  J14-8   U1-5    U2-63)
(GPD6  J14-7   U1-4    U2-62)
(GPD5  J14-6   U1-3    U2-61)
(GPD4  J14-5   U1-2    U2-58)
(GPD3  J14-4   U1-41   U2-57)
(GPD2  J14-3   U1-40   U2-56)
(GPD1  J14-2   U1-39   U2-55)
(GPD0  J14-1   U1-38   U2-54)
(GPC15     J13-8   U2-53)
(GPC14     J13-7   U2-52)
(GPC13     J13-6   U2-51)
(GPC12     J13-5   U2-50)
(GPC11     J13-4   U2-48)
(GPC10     J13-3   U2-47)
(GPC9  J13-2   U2-46)
(GPC8  J13-1   U2-45)
(GPC7  J12-8   U2-44)
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(GPC6 J12-7 U2-43)
(GPC5 J12-6 U2-41)
(GPC4 J12-5 U2-40)
(GPC3 J12-4 U2-39)
(GPC2 J12-3 U2-37)
(GPC1 J12-2 U2-36)
(GPC0 J12-1 U2-35)
(GPB15 J11-8 R33-1 S2-1 U2-34)
(GPB14 D1-1 J11-7 R34-1 U2-33)
(GPB13 J11-6 U2-32)
(GPB12 J11-5 U2-31)
(GPB11 J11-4 U2-26)
(GPB10 J11-3 U2-25)
(GPB9 J11-2 U2-24)
(GPB8 J11-1 U2-23)
(GPB7 J10-8 U2-21)
(GPB6 J10-7 U2-20)
(GPB5 J10-6 U2-19)
(GPB4 J10-5 U2-18)
(GPB3 J10-4 U2-17)
(GPB2 J10-3 U2-15)
(GPB1 J10-2 U2-14)
(GPB0 J10-1 U2-13)
(GPA15 J9-8 R29-2 U2-11)
(GPA14 J9-7 R28-2 U2-7)
(GPA13 J9-6 R27-2 U2-6)
(GPA12 J9-5 R26-2 U2-5)
(GPA11 J9-4 R25-2 U2-4)
(GPA10 J9-3 R24-2 U2-3)
(GPA9 J9-2 R23-2 U2-2)
(GPA8 J9-1 R22-2 U2-1)
(GPA7 J8-8 R21-2 U2-84)
(GPA6 J8-7 R20-2 U2-83)
(GPA5 J8-6 R19-2 U2-82)
(GPA4 J8-5 R18-2 U2-81)

(GPA3 J8-4 R17-2 U2-80)
(GPA2 J8-3 R16-2 U2-79)
(GPA1 J8-2 R15-2 U2-77)
(GPA0 J8-1 R14-2 U2-76)
(GND C1-1 C2-1 C3-1 C5-2 C6-2 C7-2 C8-2 C9-2 C10-2
C11-2 C12-2 C14-2 C15-2 C16-2 C17-2 D1-2 J1-2 J1-3 J2-2
J2-3 J2-4 J2-5 J3-2 J3-3 J3-4 J3-5 J6-2 J20-1 J21-1
J22-1 J23-1 R8-1 R9-1 R10-1 R32-2 S1-1 S1-2 S1-3 S1-4
S1-5 S1-6 S1-7 S1-8 S2-2 U1-6 U1-29 U2-8 U2-16 U2-27
U2-42 U2-49 U2-60 U3-3 U4-1 U4-3 U4-6 U4-7 U5-1 U5-3
Y2-2 Y3-2 Y4-2)
(-5A C14-1 C15-1 U3-2 U4-5)
(+6V C5-1 J1-1 U5-2)
(+5D C6-1 C8-1 C10-1 C11-1 C12-1 C16-1 C17-1 J6-1 L2-1
R7-2 R11-2 R12-2 R13-2 U1-7 U1-28 U2-22 U2-38 U2-64 U2-73
U2-78 U4-8 U5-4 Y2-1 Y2-4 Y3-1 Y3-4 Y4-1 Y4-4)
(+5A C7-1 C9-1 L2-2 U3-5)
(+5 R2-2 R33-2 R34-2)

5.6.3 Controller Wire List

(NetC40_2 C40-2 D8-1 R63-2 U9-66)
(NetC35_2 C35-2 D7-1 R55-2 U9-67)
(NetC30_2 C30-2 D6-1 R47-2 U9-68)
(NetC25_2 C25-2 D5-1 R39-2 U9-69)
(NetC20_2 C20-2 D4-1 R31-2 U9-21)
(NetJ1_2 J1-2 U14-3 U16-3)
(NetC15_2 C15-2 D3-1 R23-2 U9-20)
(NetJ1_7 J1-7 U10-3 U12-3)
(NetC10_2 C10-2 D2-1 R15-2 U9-19)
(NetJ3_7 J3-7 U5-3 U7-3)
(NetC5_2 C5-2 D1-1 R7-2 U9-18)
(NetJ3_2 J3-2 U1-3 U3-3)
(NetJ4_9 J4-9 U9-79)
(NetJ4_8 J4-8 U9-77)
(NetJ4_7 J4-7 U9-76)
(NetJ4_6 J4-6 U9-75)

(NetJ4_5 J4-5 U9-74)

(NetJ4_4 J4-4 U9-72)

(NetJ4_3 J4-3 U9-71)

(NetJ4_2 J4-2 U9-70)

(NetP1_2 P1-2 U9-45)

(NetJ?_3 J?-3 U9-9)

(NetJ2_9 J2-9 U9-5)

(NetJ2_8 J2-8 U9-6)

(NetJ2_7 J2-7 U9-7)

(NetJ2_6 J2-6 U9-11)

(NetJ2_5 J2-5 U9-13)

(NetJ2_4 J2-4 U9-14)

(NetJ2_3 J2-3 U9-15)

(NetJ2_2 J2-2 U9-17)

(NetC100_2 C100-2 U101-4)

(NetC100_1 C100-1 U101-2)

(NetD8_2 D8-2 R62-2 U17-1)

(NetD7_2 D7-2 R54-2 U15-1)

(NetD6_2 D6-2 R46-2 U13-1)

(NetD5_2 D5-2 R38-2 U11-1)

(NetD4_2 D4-2 R30-2 U8-1)

(NetD3_2 D3-2 R22-2 U6-1)

(NetD2_2 D2-2 R14-2 U4-1)

(NetD1_2 D1-2 R6-2 U2-1)

(NetR57_1 R57-1 R64-2 U17-3)

(NetR49_1 R49-1 R56-2 U15-3)

(NetR41_1 R41-1 R48-2 U13-3)

(NetR33_1 R33-1 R40-2 U11-3)

(NetR25_1 R25-1 R32-2 U8-3)

(NetR17_1 R17-1 R24-2 U6-3)

(NetR9_1 R9-1 R16-2 U4-3)

(NetR1_1 R1-1 R8-2 U2-3)

(NetC37_1 C37-1 R60-2 U17-4)

(NetC32_1 C32-1 R52-2 U15-4)

(NetC27_1 C27-1 R44-2 U13-4)

(NetC22_1	C22-1	R36-2	U11-4)
(NetC17_1	C17-1	R28-2	U8-4)
(NetC12_1	C12-1	R20-2	U6-4)
(NetC7_1	C7-1	R12-2	U4-4)
(NetC2_1	C2-1	R4-2	U2-4)
(NetC37_2	C37-2	C39-2	R59-2)
(NetC32_2	C32-2	C34-2	R51-2)
(NetC27_2	C27-2	C29-2	R43-2)
(NetC22_2	C22-2	C24-2	R35-2)
(NetC17_2	C17-2	C19-2	R27-2)
(NetC12_2	C12-2	C14-2	R19-2)
(NetC7_2	C7-2	C9-2	R11-2)
(NetC2_2	C2-2	C4-2	R3-2)
(NetC36_2	C36-2	R59-1	R61-2)
(NetC31_2	C31-2	R51-1	R53-2)
(NetC26_2	C26-2	R43-1	R45-2)
(NetC21_2	C21-2	R35-1	R37-2)
(NetC16_2	C16-2	R27-1	R29-2)
(NetC11_2	C11-2	R19-1	R21-2)
(NetC6_2	C6-2	R11-1	R13-2)
(NetC1_2	C1-2	R3-1	R5-2)
(NetC36_1	C36-1	C38-2	R58-2)
(NetC31_1	C31-1	C33-2	R50-2)
(NetC26_1	C26-1	C28-2	R42-2)
(NetC21_1	C21-1	C23-2	R34-2)
(NetC16_1	C16-1	C18-2	R26-2)
(NetC11_1	C11-1	C13-2	R18-2)
(NetC6_1	C6-1	C8-2	R10-2)
(NetC1_1	C1-1	C3-2	R2-2)
(NetR58_1	R58-1	U16-1	U16-4)
(NetR50_1	R50-1	U14-1	U14-4)
(NetR42_1	R42-1	U12-1	U12-4)
(NetR34_1	R34-1	U10-1	U10-4)
(NetR26_1	R26-1	U7-1	U7-4)
(NetR18_1	R18-1	U5-1	U5-4)

(NetR10_1 R10-1 U3-1 U3-4)

(NetR2_1 R2-1 U1-1 U1-4)

(GND C3-1 C4-1 C5-1 C8-1 C9-1 C10-1 C13-1 C14-1 C15-1
C18-1 C19-1 C20-1 C23-1 C24-1 C25-1 C28-1 C29-1 C30-1 C33-1
C34-1 C35-1 C38-1 C39-1 C40-1 C101-2 C102-2 C103-2 C104-2 C105-2
C106-2 C107-2 C108-2 C109-2 C110-2 C111-2 C112-2 C?-2 C?-2 C?-2
C?-2 C?-2 J1-1 J1-3 J1-5 J1-8 J2-1 J2-10 J3-1 J3-3
J3-6 J3-8 J4-1 J4-10 J100-2 J100-3 J?-2 P1-1 P1-3 R4-1
R5-1 R6-1 R7-1 R8-1 R12-1 R13-1 R14-1 R15-1 R16-1 R20-1
R21-1 R22-1 R23-1 R24-1 R28-1 R29-1 R30-1 R31-1 R32-1 R36-1
R37-1 R38-1 R39-1 R40-1 R44-1 R45-1 R46-1 R47-1 R48-1 R52-1
R53-1 R54-1 R55-1 R56-1 R60-1 R61-1 R62-1 R63-1 R64-1 U9-8
U9-10 U9-12 U9-16 U9-27 U9-28 U9-29 U9-30 U9-42 U9-49 U9-60
U100-1 U100-3 U101-1 U101-3 U101-6 U101-7)

(-5A C106-1 C107-1 C108-1 C111-1 C112-1 U101-5)

(-5 J1-6 J3-5 U1-2 U2-2 U3-2 U4-2 U5-2 U6-2 U7-2
U8-2 U10-2 U11-2 U12-2 U13-2 U14-2 U15-2 U16-2 U17-2)

(+6V C101-1 J100-1 U100-2)

(+6D C102-1 C?-1 C?-1 C?-1 C?-1 C?-1 L100-1 U9-22 U9-38
U9-64 U9-73 U9-78 U100-4 U101-8)

(+5A C103-1 C104-1 C105-1 C109-1 C110-1 L100-2)

(+5 J1-4 J3-4 J?-1 J?-4 R1-2 R9-2 R17-2 R25-2 R33-2
R41-2 R49-2 R57-2 U1-5 U2-5 U3-5 U4-5 U5-5 U6-5 U7-5
U8-5 U10-5 U11-5 U12-5 U13-5 U14-5 U15-5 U16-5 U17-5)

5.7 PCB Layout

The most important part of design was the PCB Layout. It was also the most frustrating. On the following pages, we have included the PCB layout of the three boards we made for senior design; the Router Board, the Controller Board, and the Selector Board:

Because of the time limitations in PROTEL, we were unable to keep using the files that we produced while we worked on the PCB layout, so the screen captures you see below are just that: screen captures from PROTEL of the boards once we had a finished layout.

If the reader has access to a working copy of PROTEL, however, he can view the files in his own version of PROTEL that are attached with this report.

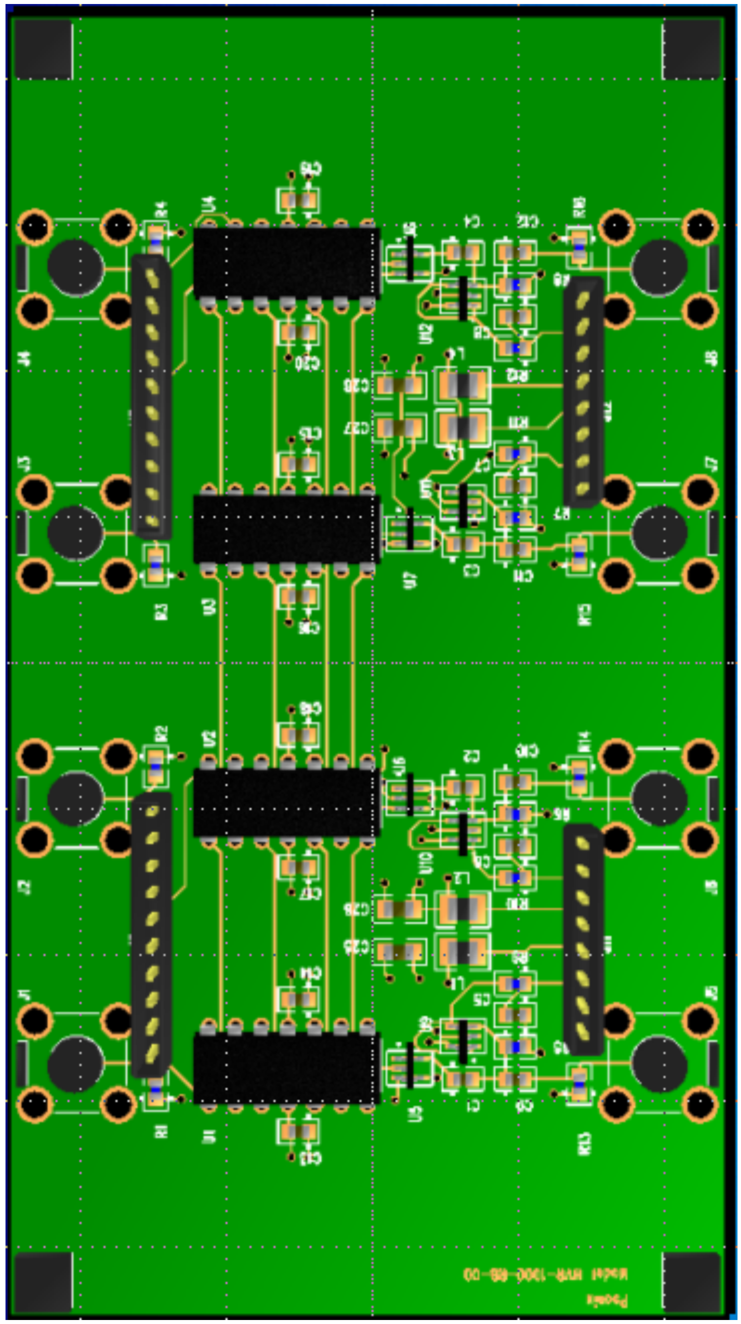


Figure 15:: Router Board PCB Layout

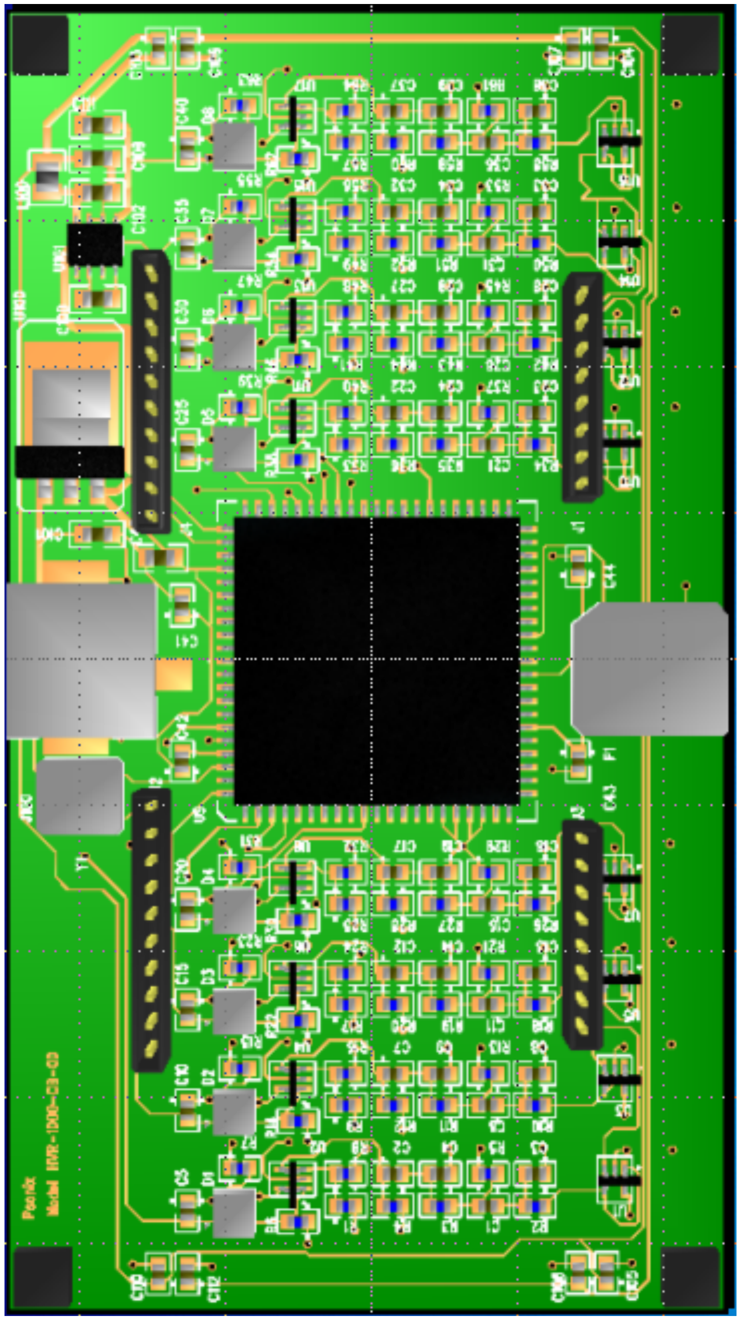


Figure 16:: Controller Board PCB Layout

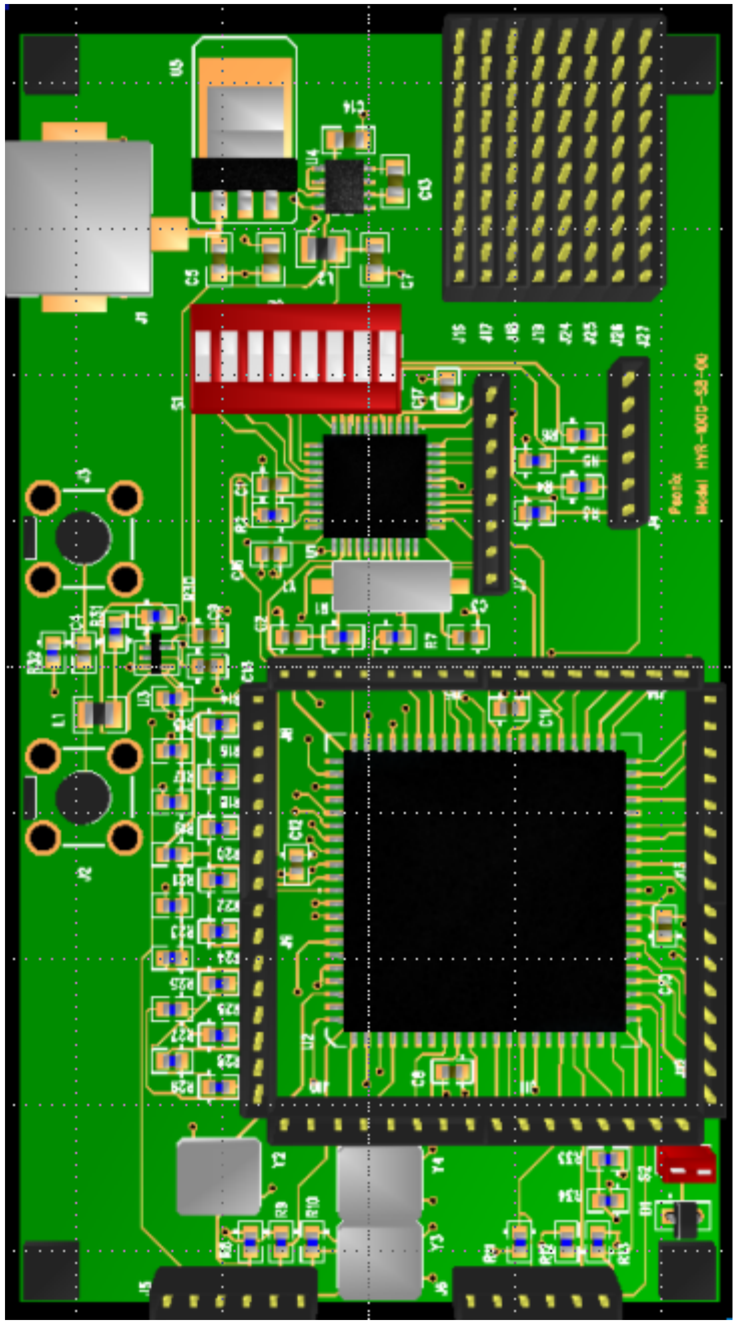


Figure 17:: Selector Board PCB Layout

5.8 Component Layout

This Component Layout from last semester details where on the prospective PC Board each of the components was going to be placed. In the figure on the following page, notice the blocks labeling what each respective space on the board is to be used for. Please note that this was not a permanent layout. We expected to make several changes to it before sending it off to the printers to be fabricated, and we did. However, this initial design is helpful in that it started us thinking about how to design our system in such a way that it is also arranged in a manner that is useful and practical.

On the following page, you will find our Component Layout and Schematic. Each place on the board is lettered to represent the part of the system that should eventually reside at that specific location on the board. We generally stayed pretty close to this first general idea; the whole product fits inside a 3"x5" silver box, and the boards are the same size as they are here, but we have changed the location of many of the individual circuit board components.

On the following pages is the initial component layout. We have added another board to the system since this iteration, labeled the controller board (you see it in the above schematics). Our design changed quite a bit, but conceptually, not all that much. Observe the changes between the PCB Layout and the Component Layout from the Spring:

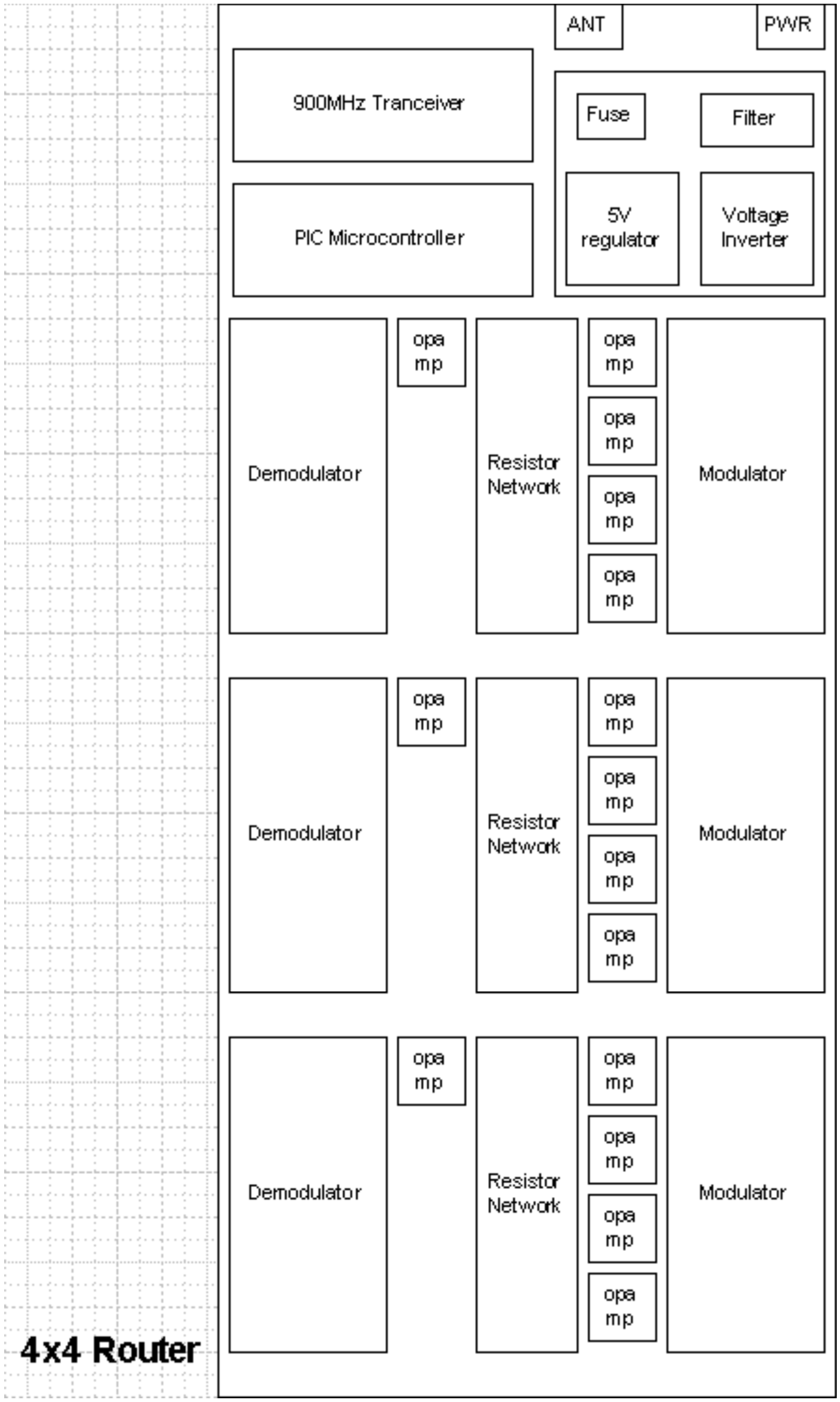


Figure 18:: HVR-1000R Component Placement Diagram

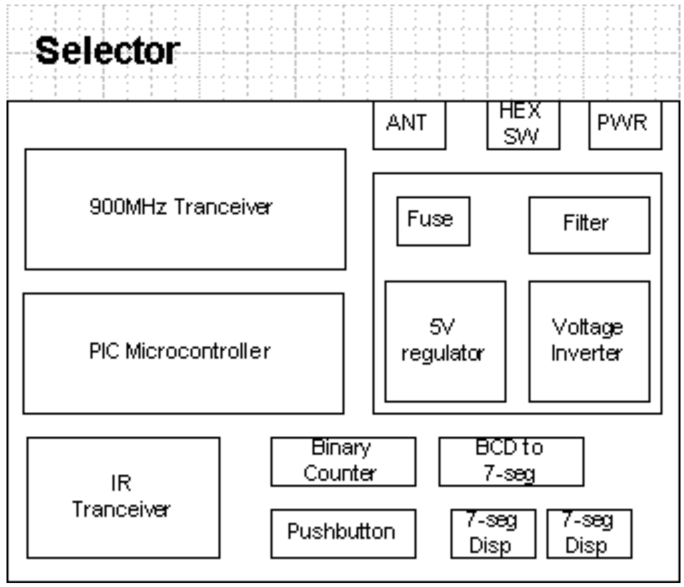


Figure 19:: HVR-1000S Component Placement Diagram

These two diagrams show the two separate parts of the system as we think they should be now. This design will change and be modified several times over the course of the next semester. Eventually, we hope to take this initial design and use it to create our PCB layout. This is scheduled to happen sometime in the next two months, although we have allowed ourselves the latitude to get it done just before the second stage of the project begins in September.

In the next section, we discuss Package Layout, and detail the appearance and look of the container that the system will eventually be put into.

5.9 Package Layout

The Package Layout is a low detail picture of what the system might typically look like. Below, you will see an image of our concept HVR-1000R and HVR-1000S in containers once the finished product is done.

We envision a smooth, metallic finish to our product, rounded edges, and a light, easy to pick up frame for each unit. On the following page, you will also see dimension specifications. These should be consistent with our original specifications. Overall, we want something sleek, fun to look at, easy to place in the average home and that will look good atop any standard television set. We hope our product will add and not detract from the appearance of the home entertainment system.

The concept system we demonstrated in lab was very close to what we envisioned the final product looking like. The silver casing is very appealing and goes well with most typical surroundings, while accommodating the entire system in a small space that is not difficult to move around or place.

Our concept is on the following page.

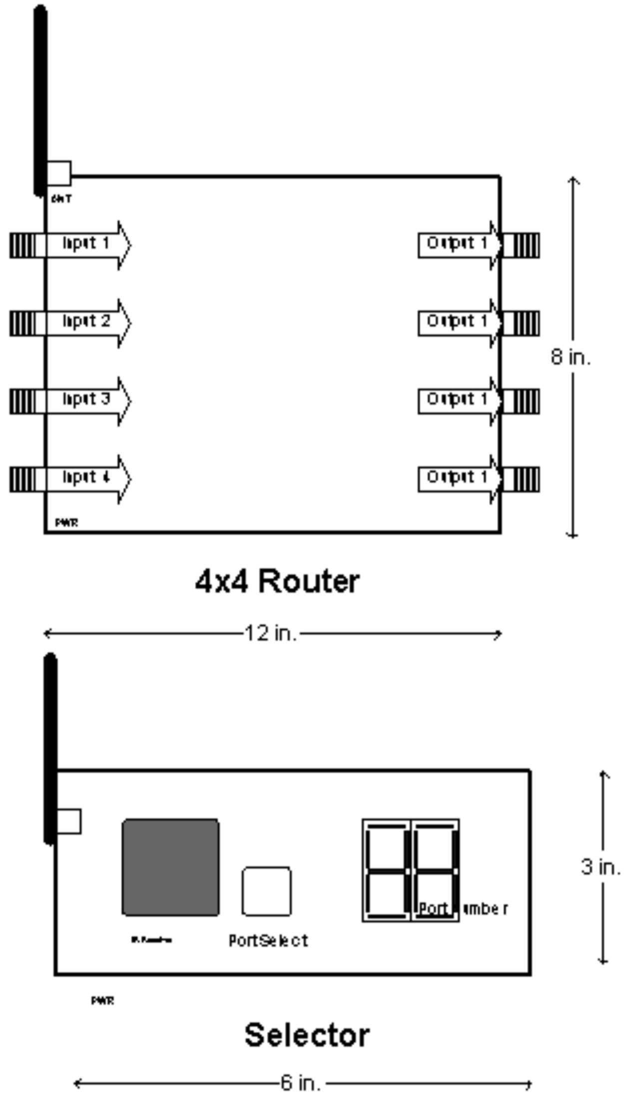


Figure 20:: HVR-1000 Package Layout

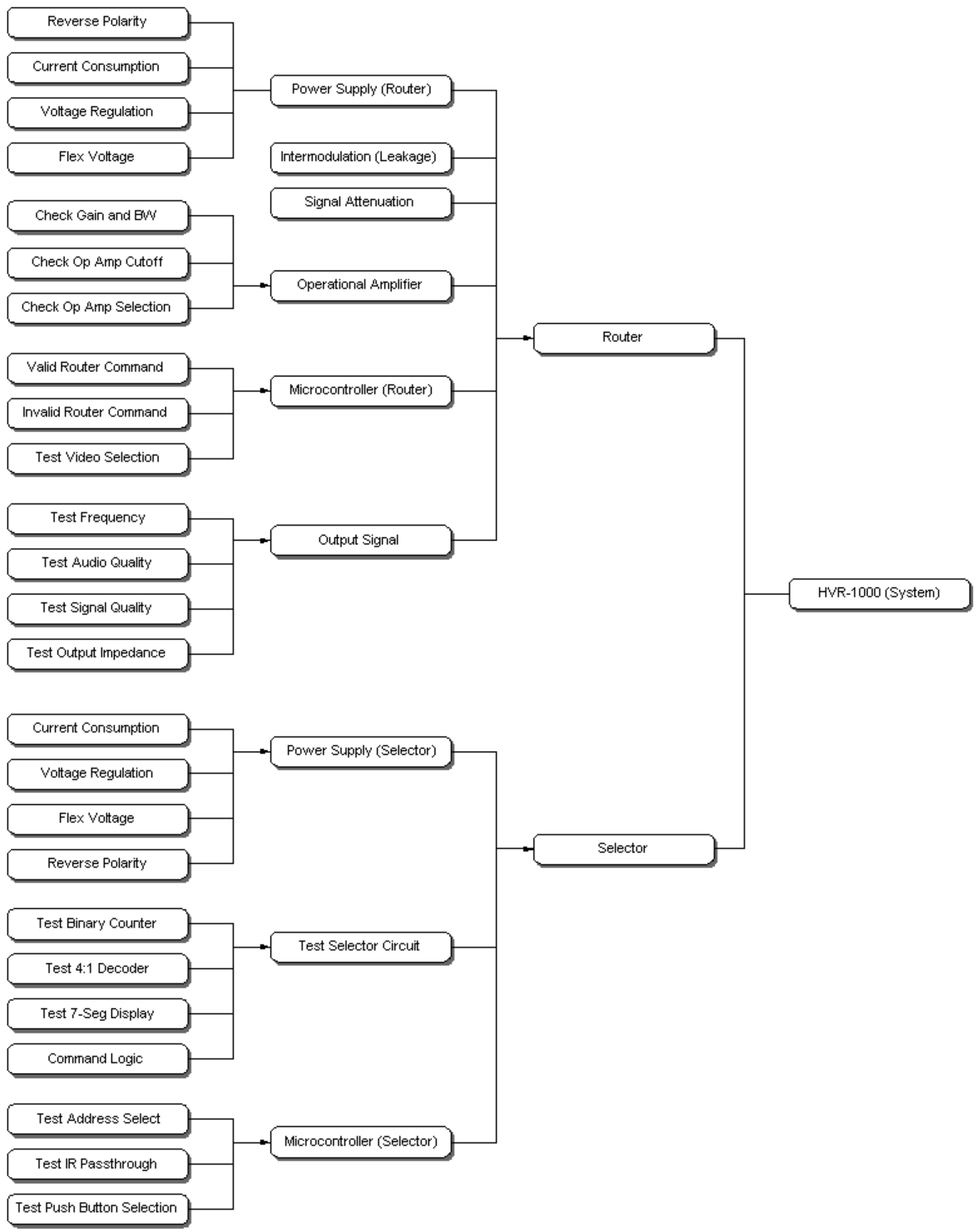
5.10 Calibration

The nature of the Psonix HVR-1000 system is such that it does not require any professional or user calibration other than the initial setup discussed in the operator's manual.

6.0 TEST SECTION

6.1 Test Flow Diagram

Below is the test flow diagram for our system, suggesting the order and types of testing to perform upon construction of the actual system.



6.2 Test Procedures

In this section, the table below offers greater detail about the various test patterns and procedures outlined in the test flow diagram from the page above. When all tests in the table are completed, the system test is made, which is described at the bottom of the table.

Device	Test Type	Procedure	Test Description	Test Equipment
ROUTER	**(Subtests)**		Verify router functionality, including signal path routing, integrity at output, current, voltage and power requirements. Verify that video appears at the output when it is selected. Verify IR and push-button command of the internal microcontroller.	Oscilloscope, DMM, Voltage Supply, Function Generator, Selector
	Power Supply	(Subtests)	Verify that the power supply at the router properly provides the subsystem with power.	Oscilloscope, DMM
		Current Consumption	Using a wattmeter, verify that the overall current consumption is within the specified range for the system.	Wattmeter
		Regulation	Verify that the voltage (from the supply) at the input of the system sits at a constant value.	Voltage Supply, DMM
		OC/SC (full load)	Test the circuit with a full load at the output under open circuit and short circuit conditions, and verify that the voltage stays constant.	Resistors (10W), DMM, Voltage Supply
		Flex Voltage	Vary power supply voltage between 11.0VDC and 13.0VDC. Verify that the video signal quality is not affected or degraded.	Voltage Supply, Oscilloscope
		Filtering	Verify that the voltage across the filtering capacitor is steady, and that minimal (nonexistent) ripple appears at the output.	Voltage Source, Oscilloscope
		Simulated Lightning Strike	Simulate a power surge (pump massive amounts of current) through the system and verify that nothing goes up in smoke.	Function Generator, Oscilloscope
		Reverse Polarity	Test the system when +/- input terminals have been reversed, and verify that no damage occurs to the system.	Voltage Supply, Oscilloscope
	Operational Amplifier	(Subtests)	Verify that the opamp matrix, once assembled and put inside the box experiences no interference, routs properly, and reacts properly to selection inputs.	Oscilloscope, DMM, Voltage Supply
		Check Cutoff	Verify that when the selector is used to change video inputs that all input op amps except the one for the desired signal are turned	Oscilloscope

			"off".	
		Check Selection	Verify that when the selector is used to select a single video input that the correct op amp is turned "on".	Oscilloscope
		Test System Gain	Verify that the system displays the correct gain value at each respective output.	Function Generator, Oscilloscope
		Test Bandwidth	Run an AC sweep (0 - 100MHz) and verify video outputs to test the full bandwidth of all op amps in the system.	Function Generator, Oscilloscope
	Intermodulation (Leakage)	(Subtests)	Verify that when the router paths are all set up at once that there is no significant intermodulation or leakage between components that might throw the entire system.	Oscilloscope, Function Generator
		Signal Transmission	Set up transmission over a single video path and check for signal interference/intermodulation on all other video paths.	Oscilloscope
		Multiple Transmission	Transmit all four signals simultaneously, and verify that a clean signal is received at each of the respective outputs.	Oscilloscope
	Signal Attenuation	Attenuation	Send a simple sine wave through the signals paths in turn, and verify the signal's amplitude at various points along the way.	Oscilloscope, Function Generator
	Output Signal	(Subtests)	Verify the integrity of the output signal at one of the specific locations. Make sure quality is not being compromised.	Oscilloscope, Function Generator
		Frequency	Check to make sure the output signal is modulated with correct carrier frequency	Oscilloscope, Function Generator
		Audio Quality	Verify that audio has been superimposed in video signal and appears at output.	Oscilloscope, Function Generator
		Signal Quality	Verify the quality of the output signal after modulation, and verify that no distortion occurs.	Oscilloscope, Function Generator
		Impedance Matching	Check each output port to verify that 75 Ohms is seen as the impedance at the output.	DMM
SELECTOR	**(Subtests)**		Verify the selector: make sure it works to select between video inputs at a given output, make certain that the voltage and power requirements are met, verify that the selector works to send commands back to the router.	Router, Function Generator, Oscilloscope, DMM
	Power Supply	(Subtests)	Verify that the power supply at the selector provides the subsystem with power.	Oscilloscope, DMM

	Current Consumption	Using a wattmeter, verify that the overall current consumption is within the specified range for the system.	Wattmeter
	Regulation	Verify that the voltage (from the supply) at the input of the system sits at a constant value.	Voltage Supply, DMM
	OC/SC (full load)	Test the circuit with a full load at the output under open circuit and short circuit conditions, and verify that the voltage stays constant.	Resistors (10W), DMM, Voltage Supply
	Flex Voltage	Vary power supply voltage between 11.0VDC and 13.0VDC. Verify that the video signal quality is not affected or degraded.	Voltage Supply, Oscilloscope
	Filtering	Verify that the voltage across the filtering capacitor is steady, and that minimal (nonexistent) ripple appears at the output.	Voltage Source, Oscilloscope
	Simulated Lightning Strike	Simulate a power surge (pump massive amounts of current) through the system and verify that nothing goes up in smoke.	Function Generator, Oscilloscope
	Reverse Polarity	Test the system when +/- input terminals have been reversed, and verify that no damage occurs to the system.	Voltage Supply, Oscilloscope
Logic Circuit	(Subtests)	Verify that the selector circuit works as a module the way it is supposed to, and verify that it correctly cycles through all inputs.	Digital Oscilloscope, DMM, Power Supply
	Counter Test	Verify that repeated depression of the debouncer switch increments the amount stored in the binary counter.	DMM, Power Supply
	Demultiplexer Test	Verify that the last two bits of the counter are passed to the demultiplexer and are interpreted correctly as a low 1-of-4.	DMM, Power Supply
	7-seg LED	Cycle through all ports (channels 1-4) via the debouncer switch, and verify that each number is displayed in turn on the 7-segment output.	DMM, Power Supply
	Logic Test	Verify that repeated depression of the debouncer switch cycles through the four input signals repetitively, and that channel numbers are displayed on the 7-seg display.	DMM, Power Supply
Microcontroller	(Subtests)	Test the microcontroller functions on board and verify that the microcontroller properly interprets inputs and controls outputs the way it is meant to.	Digital Oscilloscope, DMM

Address Selector	Verify that the microcontroller recognizes and interprets each individual selector location/address. Microcontroller must include this address information in the address byte in the wireless protocol sent to the router.	DMM, Digital Oscilloscope
IR Passthrough	Verify that the microcontroller does not interfere with remote control commands unless it requires time on the wireless interface. Verify that the microcontroller is able to interrupt IR pass through mode and master the wireless interface when it needs to send router commands.	DMM, Digital Oscilloscope
Push Button Channel Selection	Verify that the microcontroller generates a command to change inputs at the router when the debouncer switch is depressed.	DMM, Digital Oscilloscope

SYSTEM TEST: When all other tests of the individual components and subsystems are complete, verify all system requirements, including voltage, current and power requirements, verify weight and dimensions requirements, verify impedances at input and output, verify routing capability, verify signal appearance at output, verify switching speed and attenuation, verify command reception and verify user functions.

6.3 Test Results

Below is the same table of test procedures with our entered results. Each test was performed several times over the course of our design, and the end results are entered here.

Device	Test Type	Procedure	Test Description	Test Result
ROUTER	**(Subtests)**		Verify router functionality, including signal path routing, integrity at output, current, voltage and power requirements. Verify that video appears at the output when it is selected. Verify IR and push-button command of the internal microcontroller.	Router performed all functions correctly, passed signal without adding noise, met power requirements and did not visibly intermodulate.
	Power Supply	(Subtests)	Verify that the power supply at the router properly provides the subsystem with power.	Power Correctly supplied, as expected. Used 6V input to provide +5/-5V rails
		Current Consumption	Using a wattmeter, verify that the overall current consumption is within the specified range for the system.	Ammeter current shows 500 mA draw @ 5V DC
		Regulation	Verify that the voltage (from the supply) at the input of the system sits at a constant value.	Voltmeter shows +/- 5 V supply, with no flux in voltage
		OC/SC (full load)	Test the circuit with a full load at the output under open circuit and short circuit conditions, and verify that the voltage stays constant.	NOT PERFORMED
		Flex Voltage	Vary power supply voltage between 11.0VDC and 13.0VDC. Verify that the video signal quality is not affected or degraded.	NOT PERFORMED
		Filtering	Verify that the voltage across the filtering capacitor is steady, and that minimal (nonexistent) ripple appears at the output.	Supply on each plane sits at +5/-5 V.
		Simulated Lightning Strike	Simulate a power surge (pump massive amounts of current) through the system and verify that nothing goes up in smoke.	NOT PERFORMED
		Reverse Polarity	Test the system when +/- input terminals have been reversed, and verify that no damage occurs to the system.	NOT PERFORMED. Would cause device failure.
	Operational Amplifier	(Subtests)	Verify that the opamp matrix, once assembled and put inside the box experiences no interference, routs properly, and reacts properly to selection inputs.	No interference observed at video outputs.
		Check Cutoff	Verify that when the selector is used to change video inputs that all input op amps except the one for the desired signal are turned	Only one video active at a time. Works as expected.

			"off".	
		Check Selection	Verify that when the selector is used to select a single video input that the correct op amp is turned "on".	Modifications after test procedures reduce the number of op-amps to analog mux.
		Test System Gain	Verify that the system displays the correct gain value at each respective output.	Analog mux provides proper gain at output.
		Test Bandwidth	Run an AC sweep (0 - 100MHz) and verify video outputs to test the full bandwidth of all op amps in the system.	Output of analog muxes provides up to 1 dB output
	Intermodulation (Leakage)	(Subtests)	Verify that when the router paths are all set up at once that there is no significant intermodulation or leakage between components that might throw the entire system.	No intermodulation effects obvserved.
		Signal Transmission	Set up transmission over a single video path and check for signal interference/intermodulation on all other video paths.	No intermodulation effects observed
		Multiple Transmission	Transmit all four signals simultaneously, and verify that a clean signal is received at each of the respective outputs.	No intermodulation effects observed.
	Signal Attenuation	Attenuation	Send a simple sine wave through the signals paths in turn, and verify the signal's amplitude at various points along the way.	Voltage within 1dB observed at output.
	Output Signal	(Subtests)	Verify the integrity of the output signal at one of the specific locations. Make sure quality is not being compromised.	Observed signal was stable at the output ports. Small amount of intermodulation observed when not properly grounded.
		Frequency	Check to make sure the output signal is modulated with correct carrier frequency	N/A. Signal not demodulated.
		Audio Quality	Verify that audio has been superimposed in video signal and appears at output.	Video and audio are in sync, as expected.
		Signal Quality	Verify the quality of the output signal after modulation, and verify that no distortion occurs.	Small amount of distortion observed at output of router when not properly grounded.
		Impedance Matching	Check each output port to verify that 75 Ohms is seen as the impedance at the output.	Terminal load matched to both 75 and 1000 Ohms
SELECTOR	**(Subtests)**		Verify the selector: make sure it works to select between video inputs at a given output, make certain that the voltage and power requirements are met, verify that the selector works to send commands back to the	Video controls worked as expected, when modulated tone is present. Absence of modulated tone resets input to

		router.	primary.
Power Supply	(Subtests)	Verify that the power supply at the selector provides the subsystem with power.	Each ground plane is properly powed.
	Current Consumption	Using a wattmeter, verify that the overall current consumption is within the specified range for the system.	Current draw of circuit is 200 mA. Well within power supply requirements.
	Regulation	Verify that the voltage (from the supply) at the input of the system sits at a constant value.	Small voltage dip (4.91 V) observed at output of 5V regulator with full load attached.
	OC/SC (full load)	Test the circuit with a full load at the output under open circuit and short circuit conditions, and verify that the voltage stays constant.	NOT PERFORMED
	Flex Voltage	Vary power supply voltage between 11.0VDC and 13.0VDC. Verify that the video signal quality is not affected or degraded.	NOT PERFORMED
	Filtering	Verify that the voltage across the filtering capacitor is steady, and that minimal (nonexistent) ripple appears at the output.	Design modifications made after test procedures established required additional filtering for DC offset. Added Op-Amp to allow for stable output.
	Simulated Lightning Strike	Simulate a power surge (pump massive amounts of current) through the system and verify that nothing goes up in smoke.	Not tested (no fuses installed in ckt, would cause components to fail)
	Reverse Polarity	Test the system when +/- input terminals have been reversed, and verify that no damage occurs to the system.	Not tested. Would cause component failure.
Logic Circuit	(Subtests)	Verify that the selector circuit works as a module the way it is supposed to, and verify that it correctly cycles through all inputs.	Pushbutton triggers a change in frequency at the output, as expected.
	Counter Test	Verify that repeated depression of the debouncer switch increments the amount stored in the binary counter.	Works as expected.
	Demultiplexer Test	Verify that the last two bits of the counter are passed to the demultiplexer and are interpreted correctly as a low 1-of-4.	Not used.
	7-seg LED	Cycle through all ports (channels 1-4) via the debouncer switch, and verify that each number is displayed in turn on the 7-	Design modifications eliminated need for 7 segment display.

		segment output.	
	Logic Test	Verify that repeated depression of the debouncer switch cycles through the four input signals repetitively, and that channel numbers are displayed on the 7-seg display.	Design modifications eliminated need for 7 segment display.
Microcontroller	(Subtests)	Test the microcontroller functions on board and verify that the microcontroller properly interprets inputs and controls outputs the way it is meant to.	Microcontroller works as expected, no command misinterpretation.
	Address Selector	Verify that the microcontroller recognizes and interprets each individual selector location/address. Microcontroller must include this address information in the address byte in the wireless protocol sent to the router.	Replaced microcontroller code with FPGA code for simplification of project.
	IR Passthrough	Verify that the microcontroller does not interfere with remote control commands unless it requires time on the wireless interface. Verify that the microcontroller is able to interrupt IR pass through mode and master the wireless interface when it needs to send router commands.	IR Portion of project delayed to allow for PCB design. As such, no IR commands were used.
	Push Button Channel Selection	Verify that the microcontroller generates a command to change inputs at the router when the debouncer switch is depressed.	FPGA generates proper tones for detection at router.

SYSTEM TEST: As demonstrated in class, the product was more than 75% operational. However several major modifications were made that changed the scope of the project. As such, the portions of the test procedures that pertained to microcontroller code and infrared were NOT performed.

7.0 INITIAL SCHEDULE AND PROJECT COST ANALYSIS

7.1 Initial Tasks and Descriptions

Following are the initial tasks and descriptions as they existed at the end of last semester:

Task Name	Task Description
Market Research	Perform market study, research product availability, select project.
Resume	Prepare & revise personal resume.
Library Research	Research articles/documents related to the project, compare ideas.
Project/Personal Goals	Identify personal goals and combine mutual goals for the project.
Power Supply Research	Identify specifications of the power supply, discuss different power supply needs.
Power Supply Design	Design power supply specific for our project, create power supply report.
Project Status Report	Demonstrate what has been acomplished to date, compile current notes, give classroom presentation.
AM Modulator Design	Reseach and design AM modulator related to the project, discuss possible configurations or uses for modulator in relation to project.
Oscillator Design	Research, discuss and design oscillator in relation to project, decide possible locations, configurations and uses for oscillator in circuitry.
Amplifier Design	Research, discuss and design amplifier circuit, test signal path through amplifier to verify design.
Low Pass Filter Design	Research and design LPF specific to the project, discuss bandwidth needs in relation to video signals, test video transmission through LPF and verify good transmission.
Specifications	Discuss and develop list of specifications for the product, create list of marketable user features.
Functional Description	Sumurize functionality of the product, discuss product features and working project details.
Concept Diagram	Draw conceptual diagram of the product visually explaining product functionality.
IR Design	Research, discuss and design IR circuit specific to the product, test IR transmission to verify design.
Digital Selector Switch	Research, discuss and design Digital Selector Switch for the product, test selector switch to verify signal switching and design validity.
Op Amp Array Design	Research and design Op-Amp circuits for the product, design amp configuration to satisfy signal switching and routing specifications, design initial layout, build and test for design verification.
Tasks & Schedules	Create a list of detailed tasks and develop a plan/schedule for duration of tasks.
Parts Research & Availability	Research availability of parts necessary for the product, decide which parts best suit project design, begin working to develop parts list.
Theory of Operation/Selector	Summurize theory of operation for the selector, detail functionality and internal operation.
Theory of Operation/Router	Summurize theory of operation for the router, detail functionality and internal operation.
Design calculations	Perform necessary calculations to demonstrate operational specifications.
Phase Lock Loop Design	Research, discuss and design Phase Lock Loop for the product and test design to verify.
Transmitter Design	Research, discuss and design Transmiter for the selector, decide which parts to use to fulfill specifications, create initial design and test to verify design.
Digital Selector Design	Research,discuss and design digital portion of the selector, create initial design, build and test to verify design.
Assign Parts to Block Diagram	Develop a schematic that shows relationship between electrical components and sub-system blocks, detailing layout for each block.
Review and Discussion Options	Discuss problems and suggest improvements for the project
Project Parts Requirements List	Develop a complete list of parts required for the product, decide which parts are most feasible or attainable, and determine alternatives.

Request Samples	Research components necessary for the product and order samples, determine locations which offer student or other samples and apply.
Design Review Presentation	Discuss current development of the product, compile notes and give classroom presentation.
Flowchart & UI Design	Create a flowchart and UI design, detail interface functionality in relation to users, discuss signal flow and begin user manual.
Testing Plan	Develop a plan for testing the product, create list of test procedures and discuss each test step in greater detail.
Bill of Materials	Create a list of costs for the product, discuss material, component, time and space requirements, and adjust cost report accordingly.
Reordering Samples	Re-research components and re-order samples, refine list of company resources and rework required parts list.
Schematics	Create schematics for the product, define and discuss subsystems, refine project layout and connect sub-schematics.
Receiver Design	Research, discuss and design receiver for the selector, decide which parts to use to fulfill specifications, create initial design and test to verify design.
Prototyping	Design a prototype of the product, perform any soldering, wiring and/or necessary changes to create a working prototype, then test to verify system design.
Final Report	Discuss current project standing, compile notes and all previous assignments to create a report that includes complete summary of the work done on the project to date.
Software Simulation	Use software to simulate and test the design of the product, integrate microcontroller into project
Begin PCB Layout	Start designing a PCB layout to suit specifications and test using simulation software.
PCB Acquisition/Costs	Research cost and time required for the PCB fabrication.
PCB Design Review	Perform final review of the PCB design, and make any final adjustments or changes to layout.
Send Board to Fabrication	Determine best location for PCB fabrication and send fabrication order.
Build Prototypes on PCB	Test prototypes on the PCB, refine design.
Testing	Test the refined prototype of the product.
Design Review	Final review of the product.
Final Presentation	Present completed and functional product on the market.

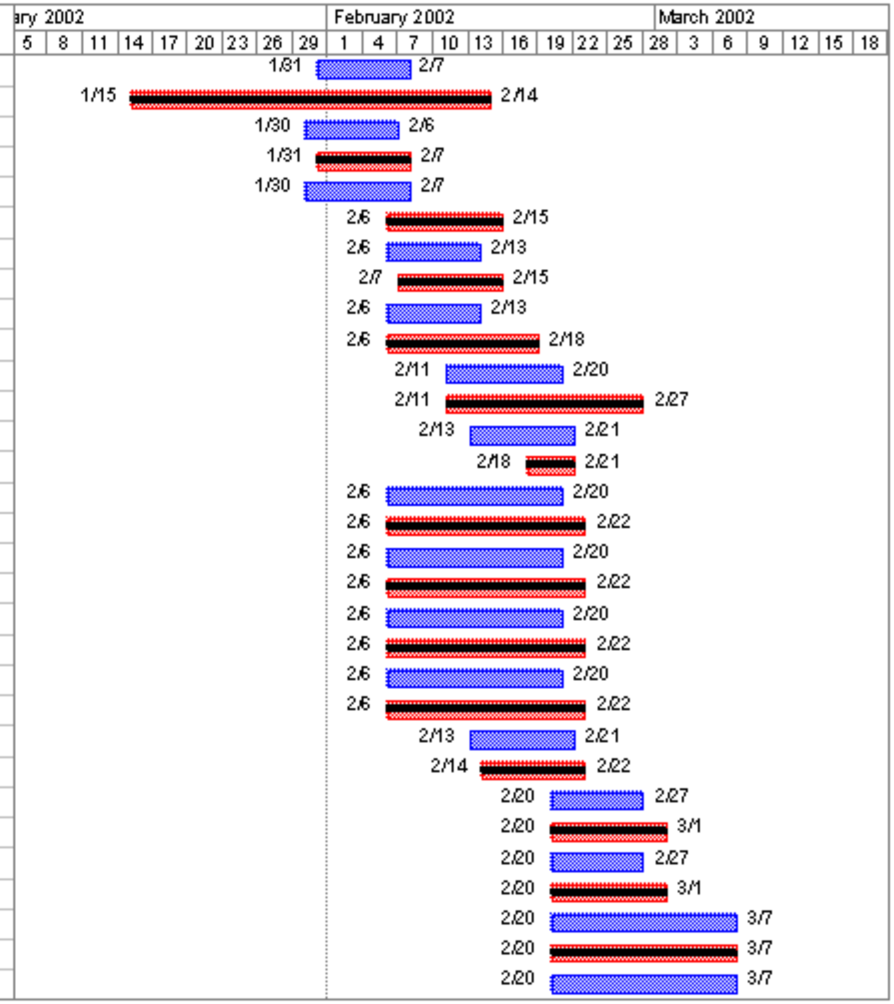
7.2 Initial Project Timeline

Below are our initial project time sheets detailing our project timeline and the processes and tasks described in section (7.1) from last semester. The project timeline spans our two project semesters and shows where each task related to the project was scheduled to occur in the first semester as well as when each task was actually accomplished. Things have changed dramatically since then and now.

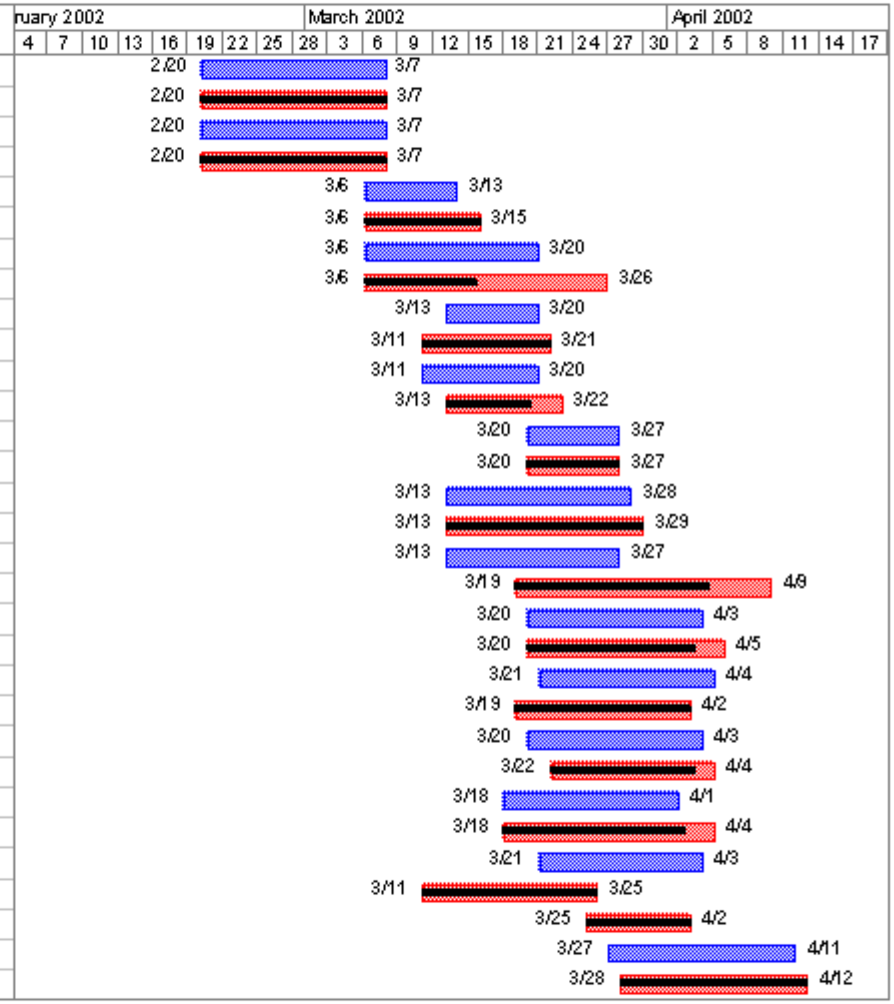
Scheduled tasks are shown in blue, and the actual task timeline is shown in red. Any discrepancies are due to problems that arose unexpectedly or specific tasks that were road blocks and that took more than their allotted time. This sort of occurrence is to be expected with any project and was not a permanent hold or stop for the group; even while some team members were grounded with specific tasks or modules that were not working, the other members were still able to move ahead and continue according to schedule.

Note that our second semester timeline was excessively short.

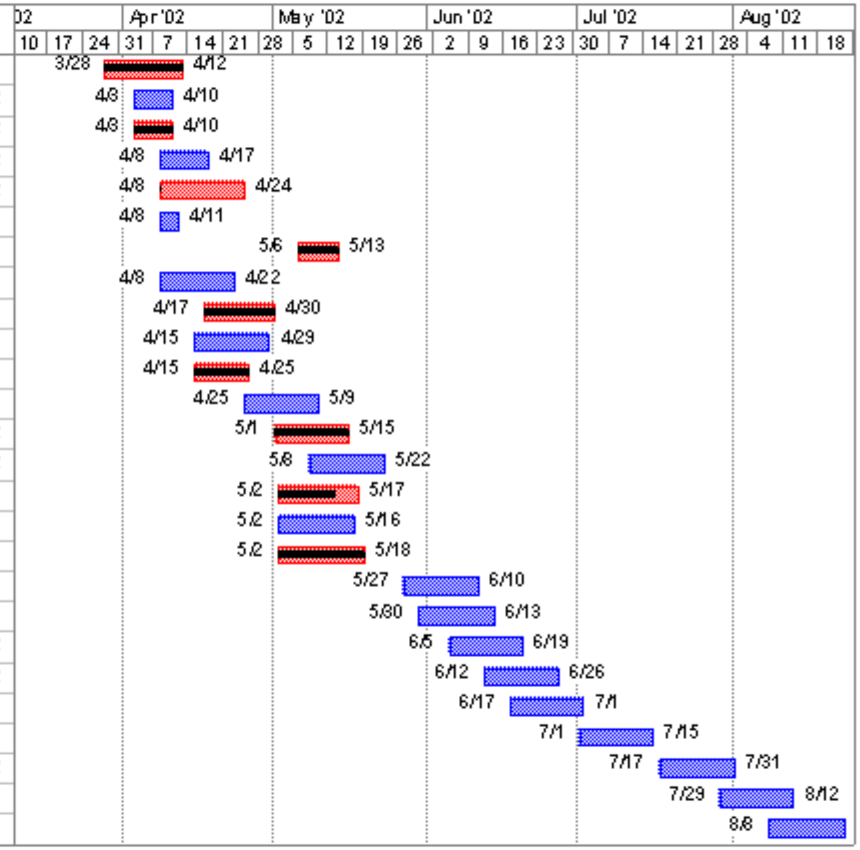
ID		Task Name	Duration	Start	Finish
1		Market Research	6 days	Thu 1/31/02	Thu 2/7/02
2	✓	Actual Market Research	23 days	Tue 1/15/02	Thu 2/14/02
3		Resume	6 days	Wed 1/30/02	Wed 2/6/02
4	✓	Actual Resume	6 days	Thu 1/31/02	Thu 2/7/02
5		Library Research	7 days	Wed 1/30/02	Thu 2/7/02
6	✓	Actual Library Research	8 days	Wed 2/6/02	Fri 2/15/02
7		Project/Personal Goals	6 days	Wed 2/6/02	Wed 2/13/02
8	✓	Actual Project/Personal Goals	7 days	Thu 2/7/02	Fri 2/15/02
9		Power Supply Research	6 days	Wed 2/6/02	Wed 2/13/02
10	✓	Actual Power Supply Researc	9 days	Wed 2/6/02	Mon 2/18/02
11		Power Supply Design	8 days	Mon 2/11/02	Wed 2/20/02
12	✓	Actual Power Supply Design	13 days	Mon 2/11/02	Wed 2/27/02
13		Project Status Report	7 days	Wed 2/13/02	Thu 2/21/02
14	✓	Actual Project Status Report	4 days	Mon 2/18/02	Thu 2/21/02
15		AM Modulator Design	11 days	Wed 2/6/02	Wed 2/20/02
16	✓	Actual AM Modulator Design	13 days	Wed 2/6/02	Fri 2/22/02
17		Oscilator Design	11 days	Wed 2/6/02	Wed 2/20/02
18	✓	Actual Oscilator Design	13 days	Wed 2/6/02	Fri 2/22/02
19		Amplifier Design	11 days	Wed 2/6/02	Wed 2/20/02
20	✓	Actual Amplifier Design	13 days	Wed 2/6/02	Fri 2/22/02
21		Low Pass Filter Design	11 days	Wed 2/6/02	Wed 2/20/02
22	✓	Actual Low Pass Filter Design	13 days	Wed 2/6/02	Fri 2/22/02
23		Specifications	7 days	Wed 2/13/02	Thu 2/21/02
24	✓	Actual Specifications	7 days	Thu 2/14/02	Fri 2/22/02
25		Functional Description	6 days	Wed 2/20/02	Wed 2/27/02
26	✓	Actual Functional Description	8 days	Wed 2/20/02	Fri 3/1/02
27		Concept Diagram	6 days	Wed 2/20/02	Wed 2/27/02
28	✓	Actual Concept Diagram	8 days	Wed 2/20/02	Fri 3/1/02
29		IR Design	12 days	Wed 2/20/02	Thu 3/7/02
30	✓	Actual IR Design	12 days	Wed 2/20/02	Thu 3/7/02
31		Digital Selector Switch	12 days	Wed 2/20/02	Thu 3/7/02



ID	Indicators	Task Name	Duration	Start	Finish
31		Digital Selector Switch	12 days	Wed 2/20/02	Thu 3/7/02
32	✓	Actual Digital Selector Switch	12 days	Wed 2/20/02	Thu 3/7/02
33		Op-Amp Array Design	12 days	Wed 2/20/02	Thu 3/7/02
34	✓	Actual Op-Amp Array Design	12 days	Wed 2/20/02	Thu 3/7/02
35		Tasks & Schedule	6 days	Wed 3/6/02	Wed 3/13/02
36	✓	Actual Tasks & Schedule	8 days	Wed 3/6/02	Fri 3/15/02
37		Parts Research & Availability	11 days	Wed 3/6/02	Wed 3/20/02
38		Actual Parts Research & Availability	15 days	Wed 3/6/02	Tue 3/26/02
39		Theory of Operation/Selector	6 days	Wed 3/13/02	Wed 3/20/02
40	✓	Actual Theory of Operation/Selector	9 days	Mon 3/11/02	Thu 3/21/02
41		Design Calculations	8 days	Mon 3/11/02	Wed 3/20/02
42		Actual Design Calculations	8 days	Wed 3/13/02	Fri 3/22/02
43		Theory of Operation/Router	6 days	Wed 3/20/02	Wed 3/27/02
44	✓	Actual Theory of Operation/Router	6 days	Wed 3/20/02	Wed 3/27/02
45		Phase-Locked-Loop Design	12 days	Wed 3/13/02	Thu 3/28/02
46	✓	Actual Phase-Locked-Loop Design	13 days	Wed 3/13/02	Fri 3/29/02
47		Transmitter Design	11 days	Wed 3/13/02	Wed 3/27/02
48		Actual Transmiter Design	16 days?	Tue 3/19/02	Tue 4/9/02
49		Digital Selector Design	11 days	Wed 3/20/02	Wed 4/3/02
50		Actual Digital Selector Design	13 days	Wed 3/20/02	Fri 4/5/02
51		Assign Parts to Block Diagram	11 days	Thu 3/21/02	Thu 4/4/02
52	✓	Actual Assign Parts to Block Diagram	11 days	Tue 3/19/02	Tue 4/2/02
53		Review & Discussion Options	11 days	Wed 3/20/02	Wed 4/3/02
54		Actual Review & Discussion Options	10 days	Fri 3/22/02	Thu 4/4/02
55		Project Parts Requirement List	11 days	Mon 3/18/02	Mon 4/1/02
56		Actual Project Parts Requirement List	14 days	Mon 3/18/02	Thu 4/4/02
57		Request Samples	10 days	Thu 3/21/02	Wed 4/3/02
58	✓	Actual Request Samples	11 days	Mon 3/11/02	Mon 3/25/02
59	✓	Spring Break	7 days	Mon 3/25/02	Tue 4/2/02
60		Design Review Presentation	12 days	Wed 3/27/02	Thu 4/11/02
61	✓	Actual Design Review Presentation	12 days	Thu 3/28/02	Fri 4/12/02



ID		Task Name	Duration	Start	Finish
61	✓	Actual Design Review Presentation	12 days	Thu 3/28/02	Fri 4/12/02
62		Flowchart & UI Design	6 days	Wed 4/3/02	Wed 4/10/02
63	✓	Actual Flowchart & UI Design	6 days	Wed 4/3/02	Wed 4/10/02
64		Testing Plan	8 days	Mon 4/8/02	Wed 4/17/02
65		Actual Testing Plan	13 days	Mon 4/8/02	Wed 4/24/02
66		Bill of Materials	4 days	Mon 4/8/02	Thu 4/11/02
67	✓	Actual Bill of Materials	6 days	Mon 5/6/02	Mon 5/13/02
68		Reordering Samples	11 days	Mon 4/8/02	Mon 4/22/02
69	✓	Actual Reordering Samples	10 days	Wed 4/17/02	Tue 4/30/02
70		Schematics	11 days	Mon 4/15/02	Mon 4/29/02
71	✓	Actual Schematics	9 days	Mon 4/15/02	Thu 4/25/02
72		Receiver Design	11 days?	Thu 4/25/02	Thu 5/9/02
73	✓	Actual Receiver Design	11 days	Wed 5/1/02	Wed 5/15/02
74		Prototyping	11 days	Wed 5/8/02	Wed 5/22/02
75		Actual Prototyping	12 days	Thu 5/2/02	Fri 5/17/02
76		Final Report	11 days	Thu 5/2/02	Thu 5/16/02
77	✓	Acutal Final Report	12 days	Thu 5/2/02	Sat 5/18/02
78		Software Simulation	11 days	Mon 5/27/02	Mon 6/10/02
79		Begin PCB Layout	11 days	Thu 5/30/02	Thu 6/13/02
80		PCB Aqusition/Costs	11 days	Wed 6/5/02	Wed 6/19/02
81		PCB Design Review	11 days	Wed 6/12/02	Wed 6/26/02
82		Send Board to Fabrication	11 days	Mon 6/17/02	Mon 7/1/02
83		Build prototypes on PCB	11 days	Mon 7/1/02	Mon 7/15/02
84		Testing	11 days	Wed 7/17/02	Wed 7/31/02
85		Design Review	11 days	Mon 7/29/02	Mon 8/12/02
86		Final Presentation	11 days	Thu 8/8/02	Thu 8/22/02



7.3 Initial Project Costs

Following are a series of tabulated sheets showing the initial assessed project costs for the year as they stood last semester. These calculated costs include not only components, parts, and materials, but they also include labor costs, equipment costs, rental costs, and working space costs for the year. Note that we also included space and labor costs for the summer months as we were working on our project through the summer.

Following, you will find, in order, tabulated material costs, electronic component costs, resource costs (including people, references, and test equipment costs), and space costs and commodities, such as office space, storage space, etc.

Total project cost for the year includes all costs for all areas and is shown at the end of the report section in bolded text. An updated look at the project budget is included in the next section, (Project Review). This section is just a reflection on the initial budget.

7.3.1 MATERIAL COST

Part Description	Vendor	Price Each	Qty	Price Total
Router				
PCB	Thomson Boards	$500.000	1	$500.000
Chasis	Fry's	$25.000	1	$25.000
F-conectors	Fry's	$2.500	8	$20.000
Selector				
PCB	Thomson Circuits	$300.000	4	$1,200.000
Chasis	Fry's	$25.000	1	$25.000
Antenna	Fry's	$3.100	1	$3.100
		Total:		**$1,773.100**

7.3.2 ELECTRONIC PARTS

Part Description	Vendor	Price Each	Qty	Price Total
Router				
FPGA	Digikey	$15.000	1	$15.000
Microcontroller	Digikey	$5.000	1	$5.000
Resistor	Digikey	$0.003	100	$0.300
Capacitor (Tantalum)	Digikey	$0.350	15	$5.250
Capacitor (Ceramic)	Digikey	$0.050	40	$2.000
Inductor	Digikey	$0.200	8	$1.600
Video OpAmp	Digikey	$0.300	20	$6.000
FET	Digikey	$0.020	16	$0.320
IR Transmitter	Digikey	$2.000	1	$2.000

900MHz Tranceiver	Digikey	$20.000	1	$20.000
Oscillator	Digikey	$0.800	5	$4.000
5V Regulator	Digikey	$2.000	1	$2.000
-5V Regulator	Digikey	$2.200	1	$2.200
3.3V Regulator	Digikey	$1.900	1	$1.900
Combo PLL/VCO	Digikey	$2.800	4	$11.200
Selector				
Microcontroller	Digikey	$5.000	1	$5.000
Resistor	Digikey	$0.003	35	$0.105
Capacitor (Tantalum)	Digikey	$0.350	5	$1.750
Capacitor (Ceramic)	Digikey	$0.050	10	$0.500
Inductor	Digikey	$0.200	2	$0.400
7-segment Display	Digikey	$0.230	3	$0.690
Binary Counter	Digikey	$0.130	1	$0.130
BCD-to-7seg	Digikey	$0.950	1	$0.950
Pushbutton Switch (debounce)	Digikey	$0.750	1	$0.750
IR Receiver	Digikey	$2.000	1	$2.000
900MHz Tranceiver	Digikey	$20.000	1	$20.000
Oscillator	Digikey	$0.800	1	$0.800
		Total:		**$111.845**

7.3.3 RESOURCE COSTS

Test Equipment	Cost	Cost/Month	Qty.	Net Cost
Equipment				
Oscilloscope	$3,995.000	$199.750	8	$1,598.000
Function Generator	$1,895.000	$94.750	8	$758.000
Power Supply	$495.000	$24.750	8	$198.000
DMM	$335.000	$16.750	8	$134.000
Test Leads	$4.950		32	$158.400
Tools				
Solder Station	$1,195.000	$59.750	8	$478.000
Solder Tips	$20.000		4	$80.000
Solder Wick	$3.800		1	$3.800
Solder	$7.000		1	$7.000
Flux	$7.150		1	$7.150
Solder Sucker	$13.500		1	$13.500
Solvent	$9.000		1	$9.000
Solvent Brushes	$2.500		2	$5.000

Anti-Static Mat	$38.000		1	$38.000
Wire-Stripper	$12.000		2	$24.000
Tweezers	$4.500		2	$9.000
Screwdriver Kit	$21.500		1	$21.500
Wire Wrap Tool	$6.500		1	$6.500
Pliers	$6.000		2	$12.000
Needle Nose	$8.000		2	$16.000
Books	$100.000		5	$500.000
Computer				
Sony VAIO FX-A47	$1,195.000	$59.750	8	$478.000
Printer	$329.000	$16.450	8	$131.600
Compiler	$75.000		1	$75.000
Emulator	$1,495.000		1	$1,495.000
ORCad	$299.000		1	$299.000
MATLAB	$499.000		1	$499.000
Programmer	$180.000		1	$180.000
		Total:		**$7,234.450**

7.3.4 SPACE/MISC. COSTS

Commodity	Cost per Unit/Month	Units	Qty.	Total Cost
Space				
Test Area	$1.200	400	8	$3,840.000
Computer Area	$1.200	256	8	$2,457.600
Storage Area	$0.600	64	8	$307.200
Miscellaneous				
Website Expenses	$18.950	1	8	$151.600
Travel Expenses	$0.350	400	8	$1,120.000
Phone	$30.000	4	8	$960.000
Postage	$0.340	5	8	$13.600
		Total:		**$8,850.000**

PROJECT GRAND TOTAL::		***$17,869.40***

8.0 PROJECT REVIEW

8.1 Project Group Goals

As a group, we were all excited about working together in team towards building a project. While we each had individual goals, which are outlined below in the next section, overall we were all interested in video routing and communications.

As such, choosing a project that fit every member of the group was not difficult. Although initially, we went through the same design considerations as the other groups, we were quickly able to settle on the video router project. Our initial goals included the use of various components that were eliminated in the second semester due to both time and technical constraints. Of these, the initial design had a wireless component for either transmitting video or router commands. This option was scratched solely because of time constraints. At the beginning of the second semester, we held a review and decided that if we wanted to have enough time to balance homework and still finish the project, we needed to eliminate the wireless portion of our design because testing and building promised to be very difficult and time consuming.

Our original goals included plans for infrared detection and forwarding in the project, but we were unable to complete this also. Infrared detection was working at the end of last semester, as the reader may have seen in project demonstrations during the last week of the Spring semester. We did not abandon the IR remote control idea, and if we take the project any further, the remote commands will definitely come into play, but for the time given, we decided that it was much more important to focus on the router and controller and get them into working shape for demonstrations as opposed to something that very much mirrored exactly our progress last semester.

One of the largest setbacks for the group was failing to account for the time we would be using to design the physical components. Initially, when we started the first semester, our goals were somewhat unclear, and at times our product verifications failed to be incorporated into our final project. In retrospect, this time could have been more effectively used towards building a more effective, and complicated product. In the end though, our final project had at times more pieces than our initial design. Several modifications made by our group allowed us to double the selector board as a development board. Instead of a generic, one time use board, we added both a FPGA, and a CPLD with JTAG interface. Additionally, we added various headers for IO, infrared, and a debounce switch. With this added functionality, we saved ourselves consider expense in the future in working with products and code.

In retrospect, although we had to change more than a few things for the design midstream, and although it may seem that we had to abandon some of our more lofty goals in favor of a lesser project that functioned, we are not discouraged. We think that we succeeded in many more important things and on a much higher level. The most important goal to all of us was to work together without conflict, and to produce a working project that all of us were happy with, and we have done that. Also, we intended to forge relationships between project members and make lifelong friendships, and we have also done that. Looking back, we think we have had a VERY successful project.

8.2 Individual Goals Review

8.2.1 Jason McLachlan

Demonstrate mastery of electronic engineering:

I wanted to be able to prove to myself that I can take an idea, generate a circuit, predict its behavior, anticipate problems, and produce a design that works as expected. I feel like I was able to accomplish this goal, and even exceed my own expectations.

Push the envelope:

I wanted to learn new things and try new ideas, regardless of what I may or may not have already known. I wanted to challenge myself to do more, think bigger, think better, and think faster. I did accomplish this goal.

Be creative:

Senior Design allowed me to imagine new things and conceive new ideas. This is something I love to do, and I certainly had the chance to do that with my senior project group. Having the time to be creative is very important to me.

Work well with others:

I wanted the experience of working with others, and concentrating on a team philosophy. I wanted to cluster ideas together, and form a strong relationship between group members. I think we succeeded in doing this, and for me, it was very gratifying to find such good friends.

8.2.2 Marck Gorszwick

Work in dynamic group

By far, largest thing I wanted to do was work on a group project with fellow engineers to build a project that I could be proud of, and responsible for. Although I've worked in an office before, the projects I've worked with have never been as large and nebulous as working on a specific product with analog and digital design.

Build communications knowledge

Since I was in my teens, I've wanted to work in communications and communications design. This project presented the opportunity to start from the ground, and design the communications portion of the project, with no rules. This allowed not only me, but the entire team plenty of leeway in deciding the signaling and control for the project.

Learn video fundamentals

This project was a good opportunity to learn about the fundamentals of video. Unfortunately, since we didn't demodulate video, I didn't learn much about video control.

8.2.3 Kat Miletijev

Explore areas of electrical engineering:

At the beginning of this project I thought that I would only work on digital portion. However, working on this project gave me an interest and insight to analog design. I have a better perspective of what I want to pursue for my career. I have definitely achieved this goal since I have a better perspective of what I want to pursue for my career and I find interest in both analog and digital design.

Gain experience of team dynamics:

Even though I have experience working in a team environment, I knew that there was still a lot to learn. I was hoping to gain good relationship with the rest of the team members and as a group to successfully complete this project. I have gained more than just a good relationship and good team experience. At the beginning of the project we were just members of the team but now we are also very good friends.

Get an insight of what it takes to be an engineer:

I wanted to get experience of what it takes to design, plan and complete a project. I knew that the project will be challenging and that there will be a lot of things that we would oversee, but with together we were able to overcome all the challenging tasks and unpredicted problems and deliver a working project. All along it was just a learning process of what it takes to be an engineer. It was definitely a good experience.

8.2.4 Austin Roundtree

Learn to work in a team:

I want to get a better idea of what it is to work in a group, have to overcome special problems with the help of other engineers, and work in tandem with people to obtain a common goal. I learned a lot with Psonix and the team members I had. We learned together, worked together, worried together, ate together, and laughed together. It was a really cool experience, and I feel like I really gained a lot from it.

Sharpen analog design skills:

I've always had an interest in analog circuitry as opposed to digital. It was my goal this semester to sharpen my analog skills and improve the way I approach the design of analog components. We definitely had the chance to design using analog in our project, and I feel that I had the opportunity to learn from my other team members while teaching them something valuable as well. I am definitely a better analog engineer because of the experience.

Improve creative problem solving skills:

Like Jason, I greatly value creativity. It was important to me at the beginning of the project to be able to offer weird alternatives as solutions and not be laughed at. Part of really good creativity is good communication, and we definitely had great communication as a project group. I feel that we approached several problems in a very creative manner, and looking back now, I am very happy to see that we have succeeded at what we set out to do.

Broaden overall knowledge of electronic design:

I really wanted to generally broaden my informational base, and I feel that I have definitely "learned a lot about a lot" during the course of this semester.

8.3 Tasks and Descriptions Review

Following is a list of updated tasks and descriptions for the second semester. Note the differences between this update and the old tasks and descriptions from last semester in the previous section.

Our task spread was much more detailed during the second semester. We as a group had a much better grasp of what it meant to make and stick to a time schedule, and we worked together much harder to obtain common goals, which, ultimately, we achieved. The tasks were one of the more frustrating parts of senior project, because we all wanted to just get up and go on the project, but as we were forced to put a schedule together and try to stay with it, we began to see the value of time allotment.

Below is the entire updated task list for the second semester. In the next section we include the project timeline in MS Project so that you can see the tasks as they relate to our time constraints.

Task Name		***Task Description***
Market Research		Perform market study, research product availability, select project.
Resume		Prepare & revise personal resume.
Library Research		Research articles/documents related to the project, compare ideas.
Project/Personal Goals		Identify personal goals and combine mutual goals for the project.
Power Supply Research		Identify specifications of the power supply, discuss different power supply needs.
Power Supply Design		Design power supply specific for our project, create power supply report.
Project Status Report		Demonstrate what has been acomplished to date, compile current notes, give classroom presentation.
AM Modulator Design		Reseach and design AM modulator related to the project, discuss possible configurations or uses for modulator in relation to project.
Oscillator Design		Research, discuss and design oscillator in relation to project, decide possible locations, configurations and uses for oscillator in circuitry.
Amplifier Design		Research, discuss and design amplifier circuit, test signal path through amplifier to verify design.
Low Pass Filter Design		Research and design LPF specific to the project, discuss bandwidth needs in relation to video signals, test video transmission through LPF and verify good transmission.
Specifications		Discuss and develop list of specifications for the product, create list of marketable user features.
Functional Description		Sumurize functionality of the product, discuss product features and working project details.
Concept Diagram		Draw conceptual diagram of the product visually explaining product functionality.
IR Design		Research, discuss and design IR circuit specific to the product, test IR transmission to verify design.

Digital Selector Switch		Research, discuss and design Digital Selector Switch for the product, test selector switch to verify signal switching and design validity.
Op Amp Array Design		Research and design Op-Amp circuits for the product, design amp configuration to satisfy signal switching and routing specifications, design initial layout, build and test for design verification.
Tasks & Schedules		Create a list of detailed tasks and develop a plan/schedule for duration of tasks.
Parts Research & Availability		Research availability of parts necessary for the product, decide which parts best suit project design, begin working to develop parts list.
Theory of Operation/Selector		Summurize theory of operation for the selector, detail functionality and internal operation.
Theory of Operation/Router		Summurize theory of operation for the router, detail functionality and internal operation.
Design calculations		Perform necessary calculations to demonstrate operational specifications.
Phase Lock Loop Design		Research, discuss and design Phase Lock Loop for the product and test design to verify.
Transmitter Design		Research, discuss and design Transmiter for the selector, decide which parts to use to fulfill specifications, create initial design and test to verify design.
Digital Selector Design		Research,discuss and design digital portion of the selector, create initial design, build and test to verify design.
Assign Parts to Block Diagram		Develop a schematic that shows relationship between electrical components and sub-system blocks, detailing layout for each block.
Review and Discussion Options		Discuss problems and suggest improvements for the project
Project Parts Requirements List		Develop a complete list of parts required for the product, decide which parts are most feasible or attainable, and determine alternatives.
Request Samples		Research components necessary for the product and order samples, determine locations which offer student or other samples and apply.
Design Review Presentation		Discuss current development of the product, compile notes and give classroom presentation.
Flowchart & UI Design		Create a flowchart and UI design, detail interface functionality in relation to users, discuss signal flow and begin user manual.
Testing Plan		Develop a plan for testing the product, create list of test procedures and discuss each test step in greater detail.
Bill of Materials		Create a list of costs for the product, discuss material, component, time and space requirements, and adjust cost report accordingly.
Reordering Samples		Re-research components and re-order samples, refine list of company resources and rework required parts list.
Schematics		Create schematics for the product, define and discuss subsystems, refine project layout and connect sub-schematics.
Receiver Design		Research, discuss and design receiver for the selector, decide which parts to use to fulfill specifications, create initial design and test to verify design.

Prototyping		Design a prototype of the product, perform any soldering, wiring and/or necessary changes to create a working prototype, then test to verify system design.
Final Report		Discuss current project standing, compile notes and all previous assignments to create a report that includes complete summary of the work done on the project to date.
Assess Market		Disscuss changes that need to be made in order to improve and simplify the project.
Update Documentation		Updat block diagrams, flow charts, and schematics for the presentations and final report.
Group Brain Storm		Implement changes to both: router and selector.
Progress Report		Evaluate current standing and progress of the project.
Tasks And Schedules		Create a list/chart of detailed tasks and develop a plan/schedule for duration of tasks.
Make Changes To Selector (BB)		Update changes made to Selector.
Make Changes To Router (BB)		Update changes made to Router.
Validate Design Changes		Validate changes. Simulate and breadboard refinements and make sure that they work.
Begin Rough PCB Layout		Initial stage of layout. Draw rough drafts of how the components will be placed on the board.
Acquire & Learn PROTEL		Acquire Protel and begin learing how to import schematics from Pspice.
Nominate Best Alternatives For Final Design		Discussed the best alternative for the simplifying/improving routher and selector design.
Set up development tools		Set up Matlab, Protel, Verilog work environment, and necessary electronic hardware.
Initial Parts Acquisition		Aquire all tools and parts that will be usend in the final project.
Acquire Necessary Development Tools		Lay the groundwork for firmware development
Begin System Breadboard		Beggin system breadboard and link numerous modules.
Finish System BB		Finish breadboarding router and selector. Beggin preparing design for the layout.
Enviromental Testing		Test how does the HVR-1000 impacts the environment.
Final System BB Review		Review the BB of router and selector. Make final changes and prepare for layout.
Finalize Hardware		Freeze schematic. Send schematic to layout.
Design Review		Outline Design Review and prepare for presentation.
Parts Pricing and Availability		Obtain majority of the parts that wiil be used for the final design. Check the prices of PCBs and return time.
Update Schematics		Replace rough scketces with scehamtics in Visio.
Begin Layout		Beggin layout for router, controller, and selector board. Take Protel tutorial and learn how to design 4 layer board.
Update Project Plan		Update project plan and schedule of tasks. Make sure we are completing tasks as planned.
Update Test Plan		Update test plan for environmental testing and layout verification.
Update Documentation		Update modified schematics such as block diagram and actual schematics of router, controller, and selectro design. Enter them in Visio/Protel.

Develop Microcontroller Code		Analyze and discuss development of Microcontroller code.
Develop FPGA Code		Develope tone generator algorithm
Integrate Analog Router		Pass video through an analog mux.
Begin Microcontroller Coding		Develop microcontroller code.
Begin FPGA Coding		Started FPGA coding.
PCB Discussion & Review		Review PCB design and begin layout for three boards.
Integrate System BB		Combine numerous modules into working one. Demonstrate that BB project works.
Research & Estimate PCB Costs		Research and compare prices of numerous vendors. Analyze and choose the best price.
Select PCB Vendor		Select PCB vendor and find out what files need to be send to the vendor for all three boards.
Testing Discussion & Review (BB)		Review BB design and start tests.
Begin System Testing (BB)		Test combined modules and improve design if needed.
Test of Op. Amp. Matrix (BB)		Test if video signal can be passed through the router matrix. Verify that two different sources can be passed and switched at the output.
Test Filtering & Bandwidth (BB)		Test BB filtering and the bandwidth and improve design as needed.
Test for Intermodulation (BB)		Test environmental set-up of the components and check for intermodulation.
Test Microcontroller (BB)		Test microcontroller code.
Test Signal Attenuation & Output (BB)		Combine modules, pass video signal through router matrix and check for the signal attenuation and noise.
Test System Logic		Test the logic of the system. Check FPGA code and microcontroller code.
Finish Testing		Finish all BB testing and prepare for the PCB layout.
Begin Selector PCB Layout		Obtain data sheets for parts, create footprints and schematic libraries for selector parts that are not included in the libraries.
Begin Router PCB Layout		Obtain data sheets for parts, create footprints and schematic libraries for router parts that are not included in the libraries.
PCB Discussion & Review		Review and discuss the status of PCB layout. Suggest the best alternative for the layout.
Finish Selector PCB Layout		Complete the selector layout and place at least 12 selector boards on the pannel.
Finish Router PCB Layout		Complete the router layout and place 4 router boards on the pannel.
Final PCB Layout Review		Final review of the PCB layout. Check connections on eash layer board, hole size, trace size, footprints, and component pins.
Final Design Review		Review the PCB layout, design, gerber files and confirm what needs to be sent to the vendor.
Verify Parts Pricing and Availability		Check the prices of FPGA, connectors, headers, and the rest of missing components that will be on PCB.
Send board to fabrication		Send board for fabrication and in the mean time work on other tasks. Ocationally check the status of the board and send any missing information or corrections to vendor.

Project Review & Update		Review project and update documentation if there are any changes.
Final Project Report Outline		Start working on Final Project Report. Turn in table of contents as a homework for the final report outline.
Update Project Plan		Update tasks and project plan. Make sure we are keeping up with the scheduled tasks.
Update Schematics		Update schematics if there are changes and replace rough scketces with scehamtics in Visio/Protel.
Update Test Plan		Update test plan for performance of the project.
Update Documentation		Update modified schematics such as block diagram and actual schematics of router, controller, and selectro design. Enter them in Visio/Protel.
Review Microcontroller Coding		Review microcontroller code and make changes if necessary.
Review Fpga Coding		Review FPGA coding and make changes if necessary.
Review System Design		Review overall system design.
Final Parts Acquisition		Aquire final parts if they haven't been ordered/obtained yet.
PCB Back From Fabrication		Receive fabricated PCB, check for errors, and implement modifications if necessary.
Build PCB Prototype (Selector)		Solder components to selector board and prepare prototype for system testing.
Build PCB Prototype (Router)		Solder components to router board and prepare prototype for system testing.
Testing Discussion & Review (PCB)		Talk about prototype test results and review prototypes in preparation for system testing.
Begin System Testing (PCB)		Bring protoboards together and begin system component testing.
Test Of Op. Amp Matrix (PCB)		Test Op Amp matrix on system router.
Test Filtering & Bandwidth (PCB)		Test all bandwidth requirements for router and/or selector.
Test For Intermodulation (PCB)		Test all signal paths for intermodulation between channels.
Test Microcontroller (PCB)		Test Microcontroller code in preparation for integration with system selector.
Test Signal Attenuation & Output (PCB)		Test all signal paths for signal attenuation at outputs, and make sure signals are not overcompensated.
Test System Logic (PCB)		Test logic circuitry on selector for ability to select between channel sources.
Finish Testing (PCB)		Place all components together for final system testing.
Finish User Manual		Finish updating User Manual for Final Project Report.
Beta Testing		Final soldering and full system test using PCB components. Give system up to a selected group of users for testing.
Marketing Review		Review marketing plan and budget to begin external marketing assessments.
Follow Up On Beta Users		Collect beta test data from all users issued an initial copy of product for testing. Gather comments and review.
Make Adjustments		Adjust final project to meet any selective criteria acquired during beta testing.
Final Design Review		Assemble and fully test the final project for functionality and usability.

Disscuss/Organize Final Presentation		Review, improve and organize previous presenation into the final one that will include pictures of the product and PCB 3D views of all three boards.
Final Presentation		Present completed project to future users.
Update/Revise Final Report		Update and complete final report. Make necessary changes/updates to the first report.
Turn in Final Report		Turn in the revised/complete final report of the HVR-1000.
Party		Celebrate the completion of the project.
Begin Pilot Build		Begin production on a larger scale using marketing indicators to choose an acceptable initial price for pilot product.
Unveil Product		Release first batch of the product to the general public.
Release Demos		Release demos to the numerous consumers.
Obtain User Feedback		Obtain feedback from users on the performance of HVR-1000.
Update Firmware, Filtering		Analyze the user feedback and update/improve firmware, filtering, and etc.
Ramp Up Production		Increase the production and review marketing of the HVR-1000.

8.4 Project Timeline & Schedule Review

During the second semester of senior design, it became much harder to adhere to a strict time schedule. In the beginning of the semester, we were able to stay close to our schedule fairly well, but in the last five weeks of design, we fell so far behind we all thought we were never going to get the project completed. Specifically, PCB layout and breadboard testing took a very long time; much longer than we expected or allowed for on the project timeline. While things looked good at the beginning, once we began to lag, other scheduled tasks lagged, and they built off of each other so that by the end of the 12^{th} week with only 4 weeks to go on the project, we were getting very worried about the outcome of the project. In the end, it was dedication and engineering power than got us through the slump.

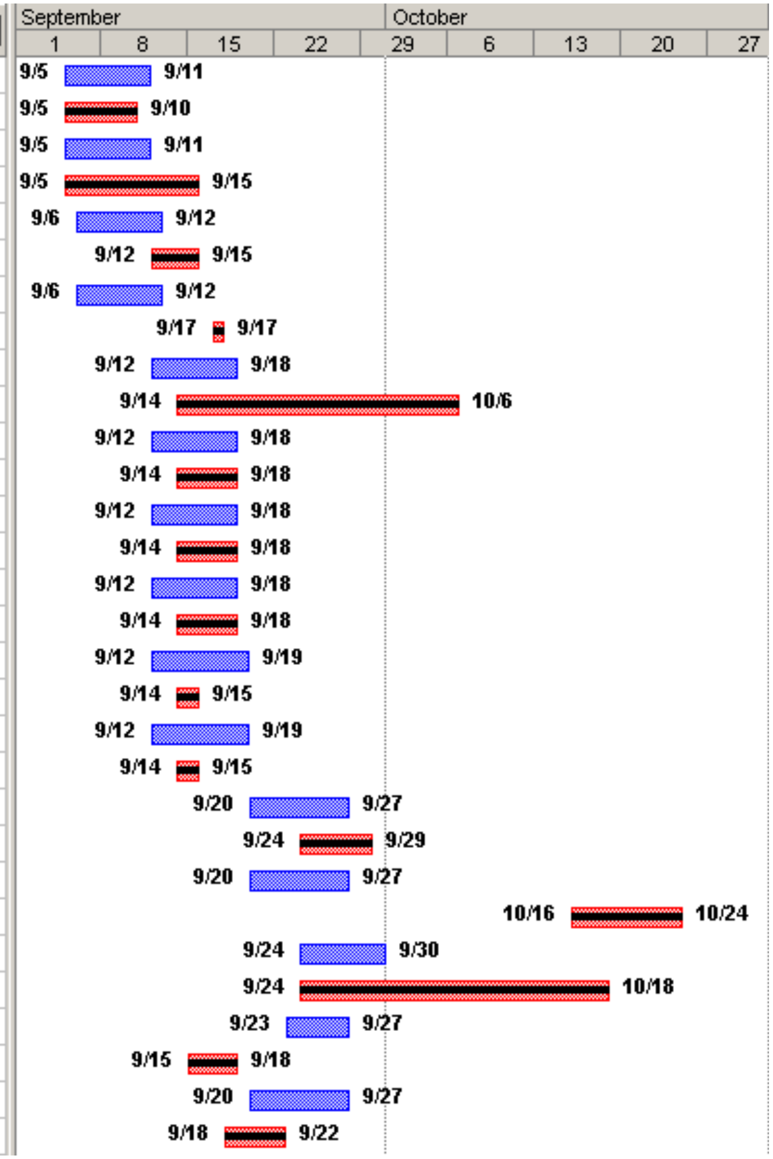
For situations like these, you will see in the timeline that there are uncommonly large schedule deviations, where several scheduled tasks overlap and run in parallel smoothly, but the actual tasks are staggered, jagged and much longer than expected. The areas where this occurred were specifically PCB layout, system testing and microcontroller coding. The reason for these deviations is the magnitude of the tasks they occurred at. The microcontroller took a long time because we saved it for last, since Jason is proficient with microcontrollers. The system testing waited for a very long time because we were having problems integrating our separate breadboards and keeping track of schematic I/O ports. PCB layout took the longest of all because we had a slough of user issues with PROTEL, the program we used for our layout.

Many of the problems we encountered during the duration of the project we found were complicated by shoddy scheduling. If more time had been spent at the beginning of the semester planning things out, we would have had a more accurate reference to look at when things went awry, and a better reference to use to get back on track. Although a pain to upkeep throughout the semester, the schedule WAS a useful tool for us, and we feel that on the next project that we do, it will be much more an integrated part of the design process.

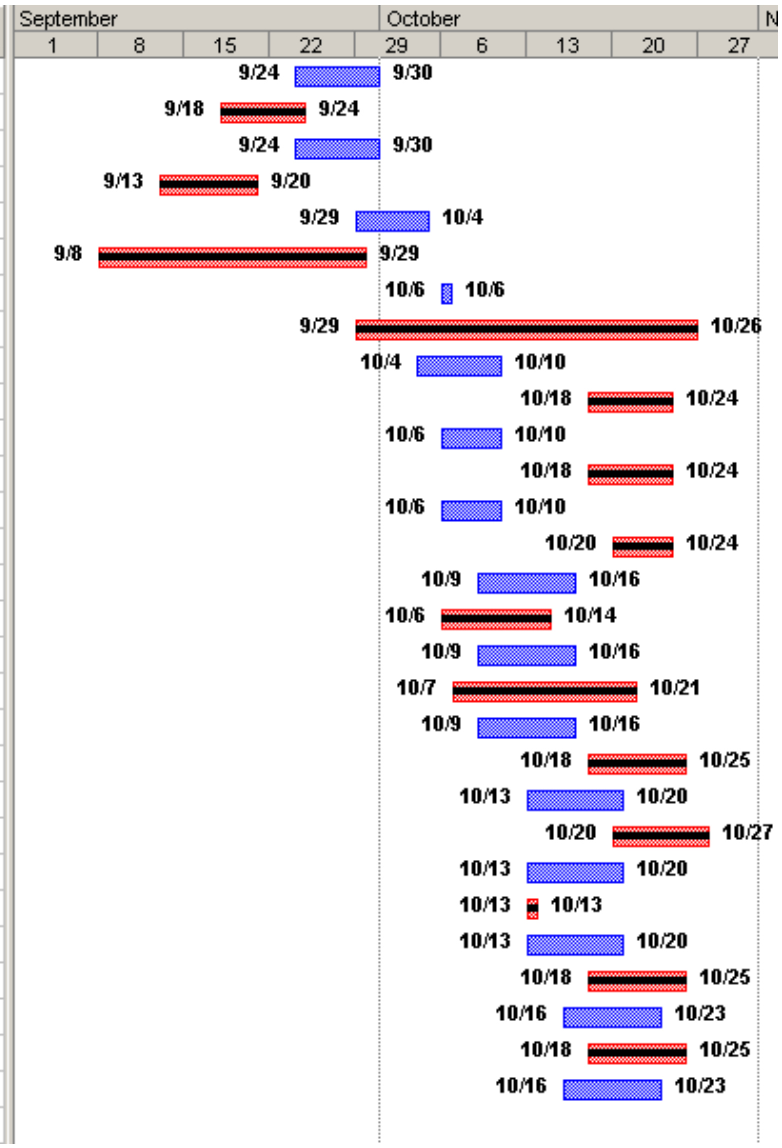
If we were to rebuild the project schedule from the ground up, there are a couple of things we would do differently. Firstly, we would get the tasks all written out early, in task blocks no greater than two weeks in length. We felt that breaking up tasks into parts less than one week in length was too much work and too difficult to do with some of the larger tasks. Secondly, we would spend a little more time earlier in the project assigning ALL tasks to specific people within the group before breaking apart to do the actual work. Thirdly, we would make a real effort to get a good program, not like MS Project that allows us to display a Gantt Chart correctly, for example, and perform some analysis functions that we could not find in MS Project. We thought the program was pretty and organizationally sound, but we would have liked to see something that sorted or displayed statistics about the project completion so far. A better option for project software might be found over the internet.

On the following pages please find the updated project timeline for the second semester of senior project.

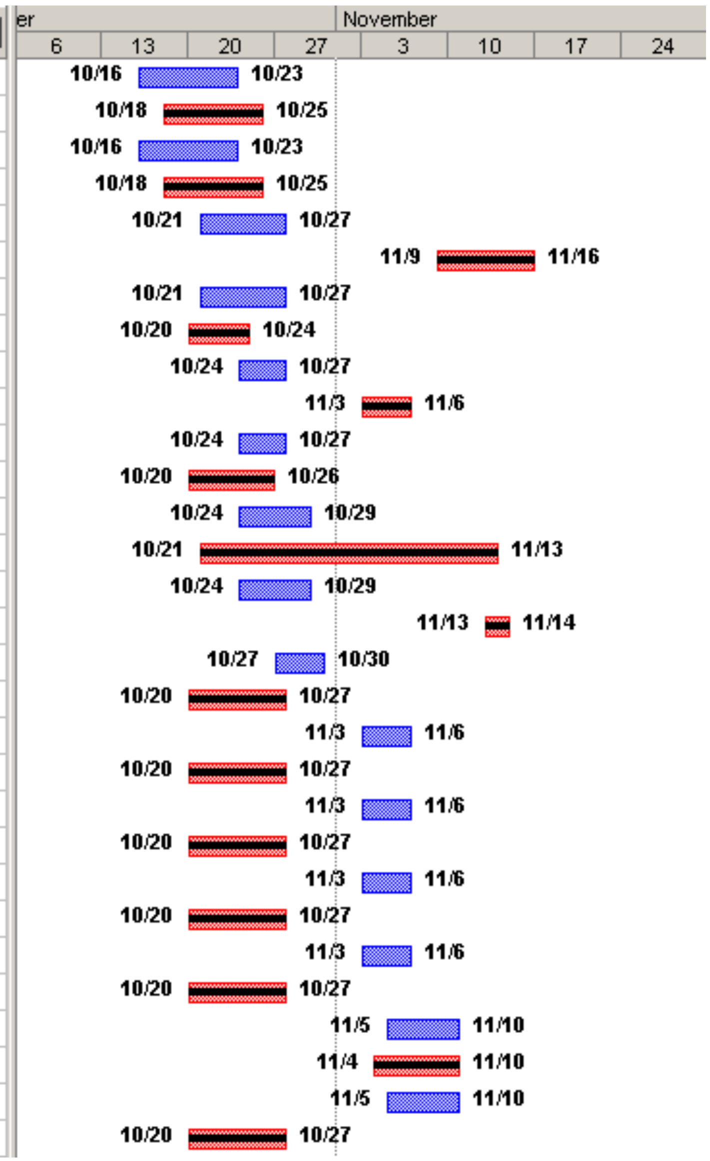
		Task Name	Duration	Start	Finish
1		Project Review & Update	6 days	Thu 9/5/02	Wed 9/11/02
2	✓	Actual	5 days	Thu 9/5/02	Tue 9/10/02
3		Project Assessment	6 days	Thu 9/5/02	Wed 9/11/02
4	✓	Actual	10 days	Thu 9/5/02	Sun 9/15/02
5		Evaluate Alternatives	6 days	Fri 9/6/02	Thu 9/12/02
6	✓	Actual	4 days	Thu 9/12/02	Sun 9/15/02
7		Assess Market	6 days	Fri 9/6/02	Thu 9/12/02
8	✓	Actual	1 day	Tue 9/17/02	Tue 9/17/02
9		Update Documentation	7 days	Thu 9/12/02	Wed 9/18/02
10	✓	Actual	20 days	Sat 9/14/02	Sun 10/6/02
11		Group Brain Storm	7 days	Thu 9/12/02	Wed 9/18/02
12	✓	Actual	5 days	Sat 9/14/02	Wed 9/18/02
13		Progress Report	7 days	Thu 9/12/02	Wed 9/18/02
14	✓	Actual	5 days	Sat 9/14/02	Wed 9/18/02
15		Tasks And Schedules	7 days	Thu 9/12/02	Wed 9/18/02
16	✓	Actual	5 days	Sat 9/14/02	Wed 9/18/02
17		Make Changes To Selector (BB)	8 days	Thu 9/12/02	Thu 9/19/02
18	✓	Actual	2 days	Sat 9/14/02	Sun 9/15/02
19		Make Changes To Router (BB)	8 days	Thu 9/12/02	Thu 9/19/02
20	✓	Actual	2 days	Sat 9/14/02	Sun 9/15/02
21		Validate Design Changes	7 days	Fri 9/20/02	Fri 9/27/02
22	✓	Actual	5 days	Tue 9/24/02	Sun 9/29/02
23		Begin Rough PCB Layout	7 days	Fri 9/20/02	Fri 9/27/02
24	✓	Actual	8 days	Wed 10/16/02	Thu 10/24/02
25		Acquire & Learn PROTEL	6 days	Tue 9/24/02	Mon 9/30/02
26	✓	Actual	22 days	Tue 9/24/02	Fri 10/18/02
27		lominate Best Alternatives For Final Desigı	5 days	Mon 9/23/02	Fri 9/27/02
28	✓	Actual	4 days	Sun 9/15/02	Wed 9/18/02
29		Set up development tools	7 days	Fri 9/20/02	Fri 9/27/02
30	✓	Actual	4 days	Wed 9/18/02	Sun 9/22/02



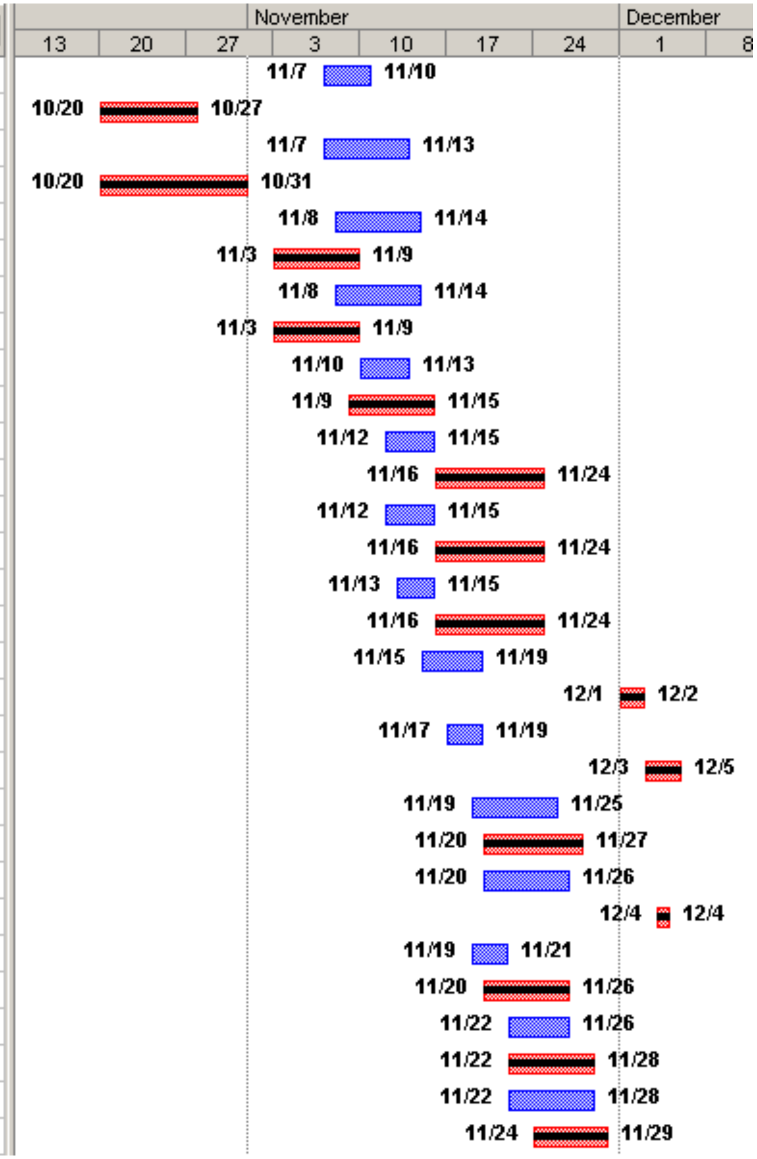
#		Task Name	Duration	Start	Finish
31		Initial Parts Acquisition	6 days	Tue 9/24/02	Mon 9/30/02
32	✓	Actual	6 days	Wed 9/18/02	Tue 9/24/02
33		Acquire Necessary Development Tools	6 days	Tue 9/24/02	Mon 9/30/02
34	✓	Actual	8 days	Fri 9/13/02	Fri 9/20/02
35		Begin System Breadboard	6 days	Sun 9/29/02	Fri 10/4/02
36	✓	Actual	20 days	Sun 9/8/02	Sun 9/29/02
37		Finish System BB	1 day	Sun 10/6/02	Sun 10/6/02
38	✓	Actual	25 days	Sun 9/29/02	Sat 10/26/02
39		Environmental Testing	6 days	Fri 10/4/02	Thu 10/10/02
40	✓	Actual	6 days	Fri 10/18/02	Thu 10/24/02
41		Final System BB Review	5 days	Sun 10/6/02	Thu 10/10/02
42	✓	Actual	6 days	Fri 10/18/02	Thu 10/24/02
43		Finalize Hardware	5 days	Sun 10/6/02	Thu 10/10/02
44	✓	Actual	5 days	Sun 10/20/02	Thu 10/24/02
45		Design Review	7 days	Wed 10/9/02	Wed 10/16/02
46	✓	Actual	8 days	Sun 10/6/02	Mon 10/14/02
47		Parts Pricing And Availability	7 days	Wed 10/9/02	Wed 10/16/02
48	✓	Actual	13 days	Mon 10/7/02	Mon 10/21/02
49		Update Schematics	7 days	Wed 10/9/02	Wed 10/16/02
50	✓	Actual	7 days	Fri 10/18/02	Fri 10/25/02
51		Begin Layout	7 days	Sun 10/13/02	Sun 10/20/02
52	✓	Actual	8 days	Sun 10/20/02	Sun 10/27/02
53		Update Project Plan	7 days	Sun 10/13/02	Sun 10/20/02
54	✓	Actual	1 day	Sun 10/13/02	Sun 10/13/02
55		Update Test Plan	7 days?	Sun 10/13/02	Sun 10/20/02
56	✓	Actual	7 days	Fri 10/18/02	Fri 10/25/02
57		Update Documentation	7 days	Wed 10/16/02	Wed 10/23/02
58	✓	Actual	7 days	Fri 10/18/02	Fri 10/25/02
59		Develop Microcontroller Code	7 days	Wed 10/16/02	Wed 10/23/02
60	✓	Actual	7 days	Sat 11/9/02	Fri 11/15/02



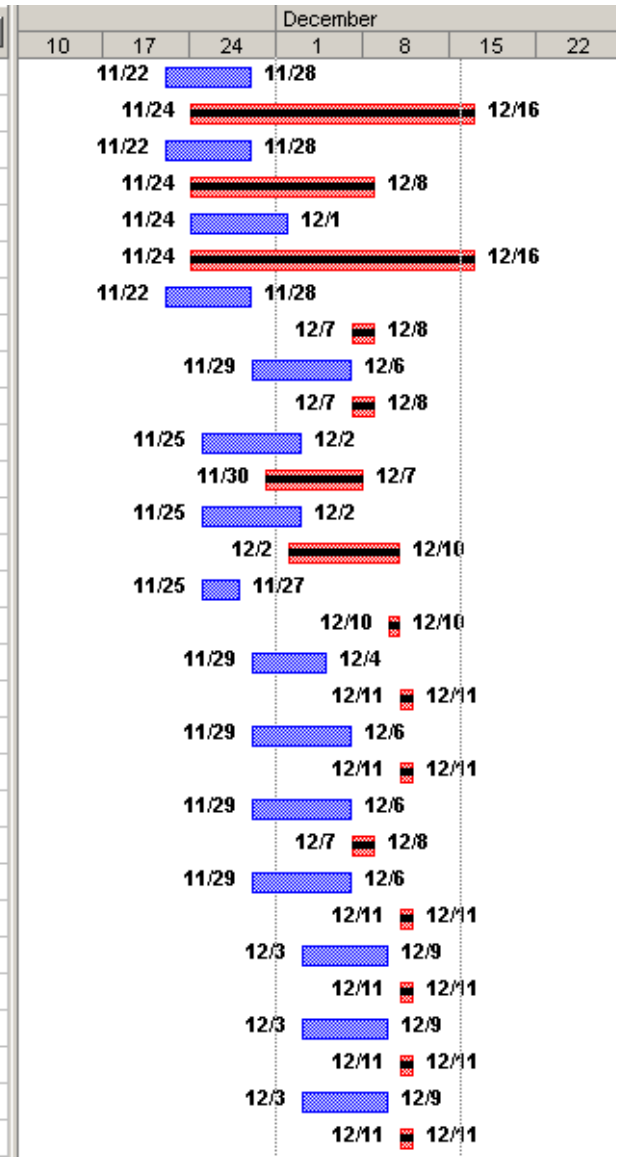
ID		Task Name	Duration	Start	Finish
61		Develop FPGA Code	7 days	Wed 10/16/02	Wed 10/23/02
62	✓	Actual	7 days	Fri 10/18/02	Fri 10/25/02
63		Integrate Analog Router	7 days	Wed 10/16/02	Wed 10/23/02
64	✓	Actual	7 days	Fri 10/18/02	Fri 10/25/02
65		Begin Microcontroller Coding	7 days	Mon 10/21/02	Sun 10/27/02
66	✓	Actual	8 days	Sat 11/9/02	Sat 11/16/02
67		Begin Fpga Coding	7 days	Mon 10/21/02	Sun 10/27/02
68	✓	Actual	5 days	Sun 10/20/02	Thu 10/24/02
69		PCB Discussion & Review	4 days	Thu 10/24/02	Sun 10/27/02
70	✓	Actual	4 days	Sun 11/3/02	Wed 11/6/02
71		Integrate System BB	4 days	Thu 10/24/02	Sun 10/27/02
72	✓	Actual	7 days	Sun 10/20/02	Sat 10/26/02
73		Research & Estimate PCB Costs	6 days	Thu 10/24/02	Tue 10/29/02
74	✓	Actual	24 days	Mon 10/21/02	Wed 11/13/02
75		Select PCB Vendor	6 days	Thu 10/24/02	Tue 10/29/02
76	✓	Actual	2 days	Wed 11/13/02	Thu 11/14/02
77		Testing Discussion & Review (BB)	4 days	Sun 10/27/02	Wed 10/30/02
78	✓	Actual	8 days	Sun 10/20/02	Sun 10/27/02
79		Begin System Testing (BB)	4 days	Sun 11/3/02	Wed 11/6/02
80	✓	Actual	8 days	Sun 10/20/02	Sun 10/27/02
81		Test Of Op. Amp Matrix (BB)	4 days	Sun 11/3/02	Wed 11/6/02
82	✓	Actual	8 days	Sun 10/20/02	Sun 10/27/02
83		Test Filtering & Bandwidth (BB)	4 days	Sun 11/3/02	Wed 11/6/02
84	✓	Actual	8 days	Sun 10/20/02	Sun 10/27/02
85		Test For Intermodulation (BB)	4 days	Sun 11/3/02	Wed 11/6/02
86	✓	Actual	8 days	Sun 10/20/02	Sun 10/27/02
87		Test Microcontroller (BB)	6 days	Tue 11/5/02	Sun 11/10/02
88	✓	Actual	7 days	Mon 11/4/02	Sun 11/10/02
89		Test Signal Attenuation & Output (BB)	6 days	Tue 11/5/02	Sun 11/10/02
90	✓	Actual	8 days	Sun 10/20/02	Sun 10/27/02



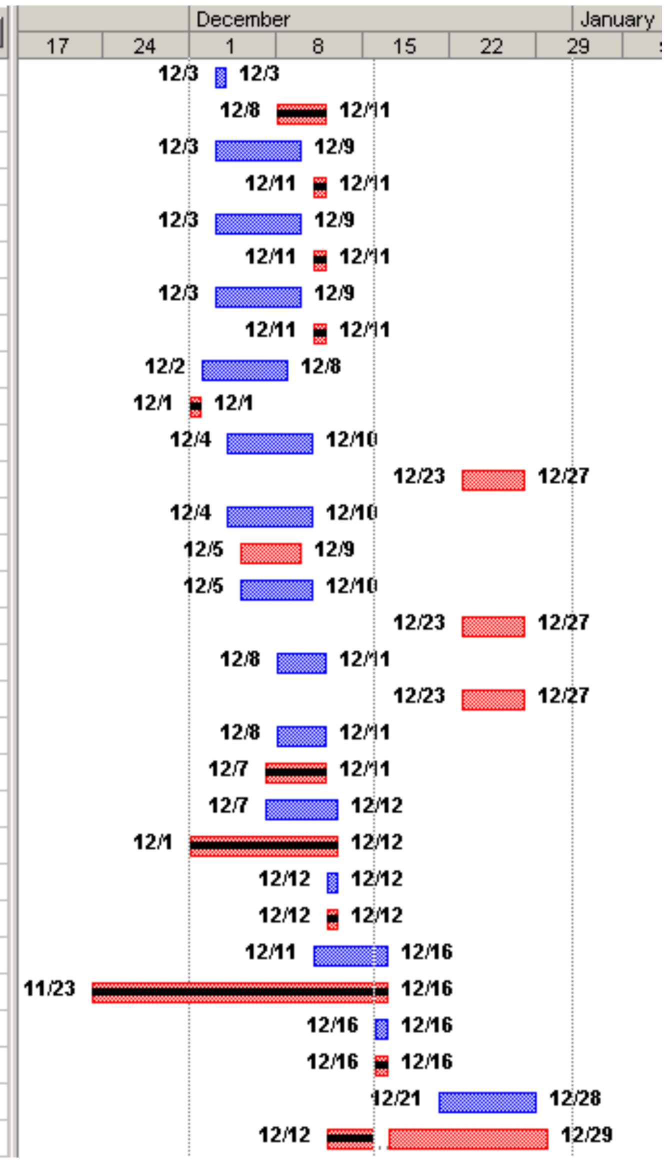
	Indicator	Task Name	Duration	Start	Finish
91		Test System Logic (BB)	4 days	Thu 11/7/02	Sun 11/10/02
92	✓	Actual	8 days	Sun 10/20/02	Sun 10/27/02
93		Finish Testing (BB)	7 days	Thu 11/7/02	Wed 11/13/02
94	✓	Actual	12 days	Sun 10/20/02	Thu 10/31/02
95		Begin Selector PCB Layout	7 days	Fri 11/8/02	Thu 11/14/02
96	✓	Actual	7 days	Sun 11/3/02	Sat 11/9/02
97		Begin Router PCB Layout	7 days	Fri 11/8/02	Thu 11/14/02
98	✓	Actual	7 days	Sun 11/3/02	Sat 11/9/02
99		PCB Discussion & Review	4 days	Sun 11/10/02	Wed 11/13/02
100	✓	Actual	7 days	Sat 11/9/02	Fri 11/15/02
101		Finish Selector PCB Layout	4 days	Tue 11/12/02	Fri 11/15/02
102	✓	Actual	9 days	Sat 11/16/02	Sun 11/24/02
103		Finish Router PCB Layout	4 days	Tue 11/12/02	Fri 11/15/02
104	✓	Actual	9 days	Sat 11/16/02	Sun 11/24/02
105		Final PCB Layout Review	3 days	Wed 11/13/02	Fri 11/15/02
106	✓	Actual	9 days	Sat 11/16/02	Sun 11/24/02
107		Finish PCB Layout	5 days	Fri 11/15/02	Tue 11/19/02
108	✓	Actual	2 days	Sun 12/1/02	Mon 12/2/02
109		Final Design Review	3 days	Sun 11/17/02	Tue 11/19/02
110	✓	Actual	3 days	Tue 12/3/02	Thu 12/5/02
111		Verify Parts Pricing And Availability	7 days	Tue 11/19/02	Mon 11/25/02
112	✓	Actual	8 days	Wed 11/20/02	Wed 11/27/02
113		Send Board To Fabrication	7 days	Wed 11/20/02	Tue 11/26/02
114	✓	Actual	1 day	Wed 12/4/02	Wed 12/4/02
115		Project Review & Update	3 days	Tue 11/19/02	Thu 11/21/02
116	✓	Actual	7 days	Wed 11/20/02	Tue 11/26/02
117		Final Project Report Outline	5 days	Fri 11/22/02	Tue 11/26/02
118	✓	Actual	7 days	Fri 11/22/02	Thu 11/28/02
119		Update Project Plan	7 days	Fri 11/22/02	Thu 11/28/02
120	✓	Actual	6 days	Sun 11/24/02	Fri 11/29/02



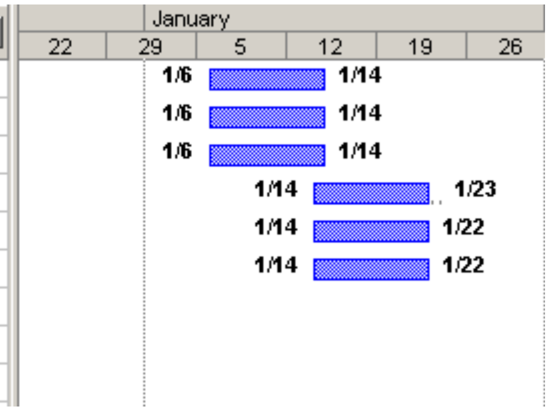
		Task Name	Duration	Start	Finish
121		Update Schematics	7 days	Fri 11/22/02	Thu 11/28/02
122	✓	Actual	21 days	Sun 11/24/02	Mon 12/16/02
123		Update Test Plan	7 days	Fri 11/22/02	Thu 11/28/02
124	✓	Actual	14 days	Sun 11/24/02	Sun 12/8/02
125		Update Documentation	7 days	Sun 11/24/02	Sun 12/1/02
126	✓	Actual	21 days	Sun 11/24/02	Mon 12/16/02
127		Review Microcontroller Coding	7 days	Fri 11/22/02	Thu 11/28/02
128	✓	Actual	2 days	Sat 12/7/02	Sun 12/8/02
129		Review Fpga Coding	7 days	Fri 11/29/02	Fri 12/6/02
130	✓	Actual	2 days	Sat 12/7/02	Sun 12/8/02
131		Review System Design	7 days	Mon 11/25/02	Mon 12/2/02
132	✓	Actual	7 days	Sat 11/30/02	Sat 12/7/02
133		Final Parts Acquisition	7 days	Mon 11/25/02	Mon 12/2/02
134	✓	Actual	9 days	Mon 12/2/02	Tue 12/10/02
135		PCB Back From Fabrication	3 days	Mon 11/25/02	Wed 11/27/02
136	✓	Actual	1 day	Tue 12/10/02	Tue 12/10/02
137		Build PCB Prototype (Selector)	5 days	Fri 11/29/02	Wed 12/4/02
138	✓	Actual	1 day	Wed 12/11/02	Wed 12/11/02
139		Build PCB Prototype (Router)	7 days	Fri 11/29/02	Fri 12/6/02
140	✓	Actual	1 day	Wed 12/11/02	Wed 12/11/02
141		Testing Discussion & Review (PCB)	7 days	Fri 11/29/02	Fri 12/6/02
142	✓	Actual	2 days	Sat 12/7/02	Sun 12/8/02
143		Begin System Testing (PCB)	7 days	Fri 11/29/02	Fri 12/6/02
144	✓	Actual	1 day	Wed 12/11/02	Wed 12/11/02
145		Test Of Op. Amp Matrix (PCB)	7 days	Tue 12/3/02	Mon 12/9/02
146	✓	Actual	1 day	Wed 12/11/02	Wed 12/11/02
147		Test Filtering & Bandwidth (PCB)	7 days	Tue 12/3/02	Mon 12/9/02
148	✓	Actual	1 day	Wed 12/11/02	Wed 12/11/02
149		Test For Intermodulation (PCB)	7 days	Tue 12/3/02	Mon 12/9/02
150	✓	Actual	1 day	Wed 12/11/02	Wed 12/11/02



		Task Name	Duration	Start	Finish
151		Test Microcontroller (PCB)	1 day	Tue 12/3/02	Tue 12/3/02
152	✓	Actual	4 days	Sun 12/8/02	Wed 12/11/02
153		Test Signal Attenuation & Output (PCB)	7 days	Tue 12/3/02	Mon 12/9/02
154	✓	Actual	1 day	Wed 12/11/02	Wed 12/11/02
155		Test System Logic (PCB)	7 days	Tue 12/3/02	Mon 12/9/02
156	✓	Actual	1 day	Wed 12/11/02	Wed 12/11/02
157		Finish Testing (PCB)	7 days	Tue 12/3/02	Mon 12/9/02
158	✓	Actual	1 day	Wed 12/11/02	Wed 12/11/02
159		Finish User Manual	7 days	Mon 12/2/02	Sun 12/8/02
160	✓	Actual	1 day	Sun 12/1/02	Sun 12/1/02
161		Beta Testing	7 days	Wed 12/4/02	Tue 12/10/02
162		Actual	5 days	Mon 12/23/02	Fri 12/27/02
163		Marketing Review	7 days	Wed 12/4/02	Tue 12/10/02
164		Actual	5 days	Thu 12/5/02	Mon 12/9/02
165		Follow Up On Beta Users	6 days	Thu 12/5/02	Tue 12/10/02
166		Actual	5 days	Mon 12/23/02	Fri 12/27/02
167		Make Adjustments	4 days	Sun 12/8/02	Wed 12/11/02
168		Actual	5 days	Mon 12/23/02	Fri 12/27/02
169		Final Design Review	4 days	Sun 12/8/02	Wed 12/11/02
170	✓	Actual	5 days	Sat 12/7/02	Wed 12/11/02
171		Disscuss/Organize Final Presentation	6 days	Sat 12/7/02	Thu 12/12/02
172	✓	Actual	12 days	Sun 12/1/02	Thu 12/12/02
173		Final Presentation	1 day	Thu 12/12/02	Thu 12/12/02
174	✓	Actual	1 day	Thu 12/12/02	Thu 12/12/02
175		Update/Revise Final Report	5 days	Wed 12/11/02	Mon 12/16/02
176	✓	Actual	22 days	Sat 11/23/02	Mon 12/16/02
177		Turn in Final Report	1 day	Mon 12/16/02	Mon 12/16/02
178	✓	Actual	1 day	Mon 12/16/02	Mon 12/16/02
179		Party	7 days	Sat 12/21/02	Sat 12/28/02
180		Actual	15 days	Thu 12/12/02	Sun 12/29/02



		Task Name	Duration	Start	Finish
181		Begin Pilot Build	7 days	Mon 1/6/03	Tue 1/14/03
182		Unveil Product	7 days	Mon 1/6/03	Tue 1/14/03
183		Release Demos	7 days	Mon 1/6/03	Tue 1/14/03
184		Obtain User Feedback	7 days	Tue 1/14/03	Thu 1/23/03
185		Update Firmware, Filtering	7 days	Tue 1/14/03	Wed 1/22/03
186		Ramp Up Production	7 days	Tue 1/14/03	Wed 1/22/03



8.5 Project Budget Review

Following are a series of tabulated sheets showing the project costs for the year. These calculated costs include not only components, parts, and materials, but they also include labor costs, equipment costs, rental costs, and working space costs for the year. Note that we also included space and labor costs for the summer months as we will be working on our project through the summer.

Following, you will find, in order, tabulated material costs, electronic component costs, resource costs (including people, references, and test equipment costs), and space costs and commodities, such as office space, storage space, etc.

Total project cost for the year includes all costs for all areas and is shown at the end of the report section in bold.

8.5.1 MATERIAL COST

Part Description	Vendor	Price Each	Qty	Actual Cost
Router				
PCB	Advanced Circuits	$33.22	3	$99.66
Chasis	Fry's	$25.000	1	$25.00
F-conectors	Molenex	Free	8	N/C
Controller				
PCB	Advanced Circuits	33.22	3	99.66
Selector				
PCB	Advanced Circuits	$33.22	12	$398.64
Chasis	Fry's	$25.000	1	$25.00
		Total:		**$647.96**

8.5.2 ELECTRONIC PARTS

Part Description	Vendor	Price Each	Qty	Price Total
Router				
FPGA	Xilinx	$11.00	4	$44.00
Microcontroller	Microchip	$5.000	1	$5.000
Resistor	AJA Video	Free	100	N/C
Capacitor (Tantalum)	AJA Video	Free	15	N/C
Capacitor (Ceramic)	Digikey	$0.050	40	$2.000
Inductor	AJA Video	Free	8	N/C
Video OpAmp	Analog Devices	$5.50	20	$110.00
Oscillator	Digikey	$4.00	5	$20.00
5V Regulator	Digikey	$2.000	4	$8.00
-5V Regulator	Digikey	$2.200	4	$8.80
Selector				
Microcontroller	Microchip	$5.000	4	$20.00
Resistor	AJA Video	Free	140	N/C
Capacitor (Tantalum)	AJA Video	Free	20	N/C
Capacitor (Ceramic)	AJA Video	Free	10	N/C
Inductor	AJA Video	Free	8	N/C
Pushbutton Switch (debounce)	Fry's	$0.750	4	$3.00
Oscillator	Digikey	$0.800	12	$9.60
		Total:		**$230.40**

8.5.3 RESOURCE COSTS

Test Equipment	Cost	Cost/Month	Qty.	Net Cost
Equipment				
Oscilloscope	$3,995.000	$199.750	8	$1,598.000
Function Generator	$1,895.000	$94.750	8	$758.000
Power Supply	$495.000	$24.750	8	$198.000
DMM	$335.000	$16.750	8	$134.000
Test Leads	$4.950		32	$158.400
Tools				
Solder Station	$1,195.000	$59.750	8	$478.000
Solder Tips	$20.000		4	$80.000
Solder Wick	$3.800		1	$3.800

Solder	$7.000		1	$7.000
Flux	$7.150		1	$7.150
Solder Sucker	$13.500		1	$13.500
Solvent	$9.000		1	$9.000
Solvent Brushes	$2.500		2	$5.000
Anti-Static Mat	$38.000		1	$38.000
Wire-Stripper	$12.000		2	$24.000
Tweezers	$4.500		2	$9.000
Screwdriver Kit	$21.500		1	$21.500
Wire Wrap Tool	$6.500		1	$6.500
Pliers	$6.000		2	$12.000
Needle Nose	$8.000		2	$16.000
Books	$100.000		5	$500.000
Computer				
Sony VAIO FX-A47	$1,195.000	$59.750	8	$478.000
Printer	$329.000	$16.450	8	$131.600
Compiler	$75.000		1	$75.000
Emulator	$1,495.000		1	$1,495.000
ORCad	$299.000		1	$299.000
MATLAB	$499.000		1	$499.000
Programmer	$180.000		1	$180.000
		Total:		**$7,234.450**

8.5.4 SPACE/MISC. COSTS

Commodity	Cost per Unit/Month	Units	Qty.	Total Cost
Space				
Test Area	$1.200	400	8	$3,840.000
Computer Area	$1.200	256	8	$2,457.600
Storage Area	$0.600	64	8	$307.200
Miscellaneous				
Website Expenses	$18.950	1	8	$151.600
Travel Expenses	$0.350	400	8	$1,120.000
Phone	$30.000	4	8	$960.000
Postage	$0.370	5	8	$13.600
		Total:		**$8,850.000**

PROJECT GRAND TOTAL::		***$16,962.81***

Excluding the non real costs (oscilloscope, salary, and non-incurred expense), our original budget was very close to what we expected it to be when we did a cursory overview of our expenses in the first semester. Initially, we expected to spend approximately $500 on a 4 layer board router board, and approximately $1200 on a selector board. In addition, we expected to spend $100 in components to build only one selector/router board.

Design modifications made to the selector and router required breaking the router into separate components – a router and a controller board. While this in turn would have normally would have increased the development costs, we instead chose to design an entire board for each team member, creating a 20"x18" sheet with 3 routers, 3 controllers, and 12 selectors. As such, the itemized costs are for the entire project, not just one board as our first semester's costs imply.

With this in mind, our overall, single board costs would be *much* cheaper if we were able to itemize the costs for an individual board. However, since the cost to manufacture the 20"x18" board were only incrementally higher than fabing three 3x5 boards, the product costs are not linear, and scaled well.

Additionally, through Jason's work we were able to procure a good deal of the electronic components (resistors, capacitors, etc), so our out of pocket costs were reduced to the PCB and active components (FPGAs, microcontrollers, oscillators, etc). By far, this saved us well over $200 in components and shipping.

Overall, our out of pocket costs for the project were around $1200. Of this, $900 was reimbursed by ASI. We will be seeking additional funding this upcoming semester to help offset the remaining costs.

8.6 The Future of the Project

While we completed a majority what we set out to, there remains several things that are yet to be done for the project. On a very superficial basis, the routing for the project works. In other words, were able to generate five separate frequencies for the tone generator and detection at the selector, however the circuitry to detect the tones at router remains unsoldered.

Additionally, we were unable to use the IR photo detector to decode commands, albeit the code is written and compiled in the FPGA. Portions of the microcontroller code (specifically that which pertains to the FPGA/IR/micro-controller action) remains yet to be written, and could thus be completed with less than one week's development time. The board itself contains headers for the IR dectectors, along with a more powerful FPGA (running at 40 MHz), so we did leave ourselves some room for future growth an expansion into adding features.

However, we failed to bring the signal to baseband, and the router lacks demodulators, so adding on screen display is not feasible with the current development board. In the future, this would be the pinnacle feature that we would like to see added – to allow the user to completely control the inputs and outputs on a per screen, digital display basis, as opposed to switching in the analog domain. While this would require some degree of signal processing, it is by no means impossible, but not feasible with the current hardware.

Overall, we are satisfied with the results of the project, and what we received in return for our efforts in producing it. Albeit in the analog domain, the video, as viewed on the remote television is sufficiently clear to prove that we did a good job of completing the project not only on schedule, but with high quality engineering design that's worthy of recognition towards one of the better senior projects this semester.

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8.7 What We Have Learned

This project has been very beneficial for the whole group. Our goal was to gain experience in working with others, and concentrate on team dynamics. In this project, we learned not only how to share knowledge, but how to incorporate different ideas into the project. While working in the group, we formed a strong relationship with each other and we have plans to continue working as a team in the future. This project gave us an opportunity to create a working design with zero foundation, and build a working project. All four members of the team were challenged by the project, and all of us had a chance to be creative and create new ideas. In all, we all have learned more about different areas of electronics.

Senior Design Project, as a class, gave us an insight of all aspects that make a complete project. The amount of documentation, detailed graphs, schematics, numerous reports, and numerous presentations formed the collective sum of our work. Not only did this class give us insight into what it takes to be an engineer, but also gave us the knowledge about the responsibilities that come with being an engineer. During the last 10 months, we learned new software and we put our engineering curriculum coursework into practice.

If we had a change to work on the project all over again, the largest thing we would change would be our management of time. Additionally, we should have learned Protel earlier. Lastly, we would recommend to any future senior project classes, that the take advantage of the free time during their summer/winter breaks.

The most significant contribution that we received from this class was the development board that we designed as part of the project. With this board, we can no only add more features to the video router, but we can double it for any future engineering tasks that come up. Future enhancements that we can make include adding infrared detection, on screen display, and remote control forwarding.

One of the things we would keep the same is team dynamics. We would still make sure that each member works on all parts of the project since that way all of us will gain experience in different areas. One of the things we definitely need to work on is time management and give much more time to learning new software.

8.8 Internal Individual Evaluations:

8.8.1 Jason McLachlan's Group Evaluations

I am proud to say that everyone in my group performed responsibly and to the best of their abilities. Throughout the journey of Senior Design, we encountered many challenges together as a group. We stood up to those challenges, and my fellow group members helped drive this project to the finish line. Our diverse backgrounds, willingness to succeed, and friendship allowed us to follow through with a project from start to finish. Our group took the initiative to insure that the elements of our design were finished on time and as planned. After about a dozen pizzas, 15 lbs. of peanut M&Ms, at least 25 trips to Grass Valley, my dedicated team members succeeded in meeting their goals as individuals, and as a group. We succeeded in producing a working product that was just a dream 10 months ago. Everyone's good sense of humor and high spirits will never be forgotten.

Katarina (Kat) Miletijev:

Kat's hard work and dedication as a team member is a quality that will carry her well into her future career. Coupled with her organizational skills and determination, she kept the team on track, and focused on what was important for Senior Design. She added dynamics to our group, and was also able to put up with the rest of us obnoxious guys.

Marck Gorszwick:

Marck's natural abilities, ingenuity, and experience working with technology gave our group the added mechanism of good feedback on new ideas. He is very opened-minded, and always keeps you thinking. He is quick to answer any questions, and seems to know a lot about everything.

Austin Roundtree:

Austin's ability to crunch numbers and desire to learn allowed him to quickly put together new concepts and apply them in practice. He is very efficient and can build things exactly as desired. He is very good at following schematics, soldering, and building prototypes perfectly the first time around.

Jason McLachlan:

I believe that my performance in this project has been excellent. I've shown my dedication to the project and to the team by staying up numerous night trying to solve the problems we encountered. Additionally, I believe that my experience and my knowledge led to successful completion of the project.

8.8.2 Marck Gorszwick's Group Evaluations

Whilst this hath been a much filled semester, with many a design review, and many a voyage to Grass Valley to complete the system design, the overall project a success it was. Several nights have passed where the entire team worked through the night to get things done, and each member is deserving of an honorable mention towards making the end project a success.

The Most Esteemed Jason McLachlan:

Jason is a god. Well, maybe not a god, but at least a minor deity. Without Jason's engineering knowledge, perseverance, and tenacity towards completing the project, we would have surely failed. Jason is wholly responsible for nearly every performance tweak and modification to make sure the project worked as planned. When something didn't work, or we needed an alternative to a problem, Jason was the first to offer an alternative, and explain why his ideas were better or worse than our proposition.

Mr. McLachlan deserves nothing less that the highest mark for the project.

The Honorable Austin Roundtree:

Austin, while at times a bit off humor, provided the steam and driving force for the project. Whenever we needed motivation, and pep, Austin forged forward, giving us a reason to push ahead towards completing the task de jour. Besides his uncanny ability to keep us motivated, Mr. Roundtree also possesses countless engineering talents that we heartily used over the course of the last year. His contributions in working with the counters, frequency generation, and PCB place him on equal footing with Mr. McLachlan in both technical prowess and group motivation.

Mr. Roundtree also deserves the highest marks for the project.

Her Lady, Katarina Miletijev

Katarina, or Kat as know by everyone in Engineering, gave our group the constant reminders that we were behind schedule, and needed to catch up to complete the project. When not working on the project timeline, Kat contributed heavily to the conceptual design of the filter network, and the control section for the router. In the first semester, she did a significant amount of work on VCOs and PLLs, even though these were not used significantly.

Miss Miletijev deserves high marks for her participation in the project.

Marck Gorszwick:

This past year has been an incredible learning experience for me. In it, I've had the opportunity to gain so much engineering knowledge, and learn not only about professional team dynamics, but also build a good network of close-knit friends. In comparison to the others in the group, I feel as though my performance hasn't quite equaled Jason, Austin, or Kat's, even though what I've learned in general about engineering is parallel to theirs.

I feel as though I deserve above average marks for my participation.

8.8.3 Kat Miletijev's Group Evaluations

What is there to say except I never expected that my experience in senior design project would be so awesome! It was great working with the guys, but what is more important is that we became very good friends. We spent so many nights working on the project and even then we were able to laugh and have fun. It was great to see that all four of us were willing to change our plans so that we can meet and complete our tasks on time. Sometimes our schedules conflicted, but we never complained if it was three, two, or just one of us working on the project. Every other weekend, and towards the end every weekend, Austin, Marck, and I would drive to Grass Valley to meet with Jason. We would split tasks and then switch so that all of us could gain experience with every portion of the project. Every member of our team had different qualities, and when combined together we were able to enjoy working on the project and overcome any difficulties.

Jason McLachlan:

Jason's dedication to the project and to the team was absolutely incredible! For every encountered problem, Jason stayed up day and night until he figured out the solution. We all wanted to learn a lot from this project, but most of the things that I learned during past 10 months were from Jason. He is extremely smart individual and without his hard work it would have taken much longer to complete this project.

Marck Gorszwick:

Marck finds interest in everything. He asks a million questions, he wants to learn, and he is always ready to give an alternative to improve the design. His dedication, abilities, and experience in technology were very helpful to the project. Not only was he efficient in working on numerous task at the same time, but he definitely added dynamics to our team.

Austin Roundtree:

Austin's ability to memorize things and learn new concepts with little reference was extremely beneficial to our project. He is very efficient in every task he performs, and completes each one meticulously. Austin is a dedicated individual, and will often over exert himself to make the task at hand successful.

Katarina Miletijev:

One of my best skills is making sure we completed tasks on schedule. My organizational skills, dedication to the project, and hard work definitely impacted the team and the project. Not only was I always open to learning new things, but I always completed the tasks for which I was responsible. There are things that I could have done better, but overall I believe my performance in this project was excellent.

8.8.4 Austin Roundtree's Group Evaluations

I am happy to say that Psonix's team members came, designed and conquered to the best of their abilities. We came across a thousand different hitches and problems in the design over the last year, but with hard work and perseverance from everyone, we overcame those obstacles and produced a project that shone. Everyone on the team had a fantastic drive to attain the goals they set, and the ambition to set the goals in the first place. The trips to Grass Valley, although long and arduous, were worth every minute. The long sleepless nights pulling things together at the last minute have paid off after all. The friendships I made during senior project are there forever, and the memories I have will last a very long time indeed.

Jason McLachlan:

Jason is a real engineer. I looked up to Jason through the whole of senior design. Every time there was a problem that seemed unbeatable, we looked to Jason for comfort, and eventually, a solution. Jason's sheer ability to sit down and focus his thinking and get the job done is astounding. His willingness to sacrifice almost anything for the sake of the team and the sake of the project has seen us through. This team would have been nothing without him.

Katarina (Kat) Miletijev:

Kat put up with a lot from all of us, while we poked fun at her mercilessly and gave her a hard time about everything from her accent to the way she ate pizza. All in all, though, Kat is a very hard worker, a good engineer, as steady as a rock when you need to rely on her, and a wonderful friend. I would not part with a bit of her expertise or talent.

Marck Gorszwick:

Marck is good at everything. There isn't a subject that he can't tell you something about, and I found his resourcefulness to be absolutely essential to the group. He regularly made the effort to participate and contribute to the project, giving feedback or suggestions when the rest of us were stumped. I value Marck's contribution to the project greatly.

Austin Roundtree:

I don't know what to say about myself but that I felt like I fit within this group. Everything I feel for these people on my team I know they feel about me too. Looking back, I know that I gave it all I had. I did my part for the team, and I know that I am appreciated for it, just as I in turn appreciate Kat, Marck and Jason for all their hard work. In the end, I am grateful to have made such friends, and I am happy to have spent the time that I did in their company.

APPENDIX A: DATASHEETS/Attachments

Please follow these links to view datasheets for those electrical components that are most pertinent to our project, the HVR-1000.

LM2662/LM2663 Switched Capacitor Voltage Converter

MIC29150/29300/29500/29750 Series
High-Current Low-Dropout Regulators

PLCC (PC20, PC28, PC44, PC68, PC84) FPGA

PIC16C6X Microcontroller

RASM722 – Power Jack, Surface Mount

Molinex F-Connector

Samtech Headers

AD8051/AD8052/AD8054
Low Cost, High Speed
Rail-to-Rail Amplifiers

750 MHz, 3.8 mA
10 ns Switching Multiplexers
AD8180/AD8182*

Gerber Files for PCB

Group & PCB Photos

APPENDIX B: RESOURCES

Lathi, B.P. <u>*Modern Digital And Analog Communication Systems, 3rd Ed.*</u>
Oxford University Press; New York. (1998)

Sedra and Smith. <u>*Microelectronic Circuits, 4th Ed.*</u>
Oxford University Press; New York. (1998)

Valkenburg, Van. <u>*Analog Filter Design.*</u>
Oxford University Press; New York. (1998)

Hudson & Luecke. <u>*Basic Communications Electronics.*</u>
Master Publishing, Inc; Lincolnwood, Illinois. (1999)

Oppenheim, Alan. <u>*Discrete-Time Signal Processing.*</u>
Prentice Hall; Upper Saddle River, NJ. (1999)

Nise, Norman S. <u>*Control Systems Engineering.*</u>
John Wiley & Sons; New York. (2000)

<u>*The ARRL Handbook for Radio Amateurs.*</u> *79th Ed.*
National Association for Radio Amateurs; Newington, CT. (2001)